Design and Analysis of Key Components for Manufacturable and Low-Power CMOS Millimeter-Wave Receiver Front End

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Design and Analysis of Key Components for Manufacturable and Low-Power CMOS Millimeter-Wave Receiver Front End

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3G	3rd generation; 3rd generation of mobile telecommunications technology
4G	4th generation; 4th generation of mobile telecommunications technology
ADC	analog-to-digital converter
ADS	Agilent Technologies' Advanced Design System
β	current gain
BB	baseband
BEOL	back end of line
BER	bit error rate
BiCMOS	Bipolar CMOS technology
BJT	bipolar junction transistor
BPSK	binary phase-shift keying
C	capacitor
CC (code)	convolutional code
CC (topology)	cascode
CC-VCO	cross-coupled VCO
CG	common-gate
CMOS	complementary metal-oxide semiconductor
CPW	coplanar waveguide
CS	common-source
E-band	71-76 and 81-86 GHz frequency band
ECMA	European Computer Manufacturers Association
EIRP	equivalent isotropically radiated power
EM	electromagnetic
ESD	electrostatic-discharge
ESR	equivalent series resistance
ETSI	European Telecommunication Standards Institute
f_c	flicker noise corner frequency
FCC	federal communication commission
FET	field-effect transistor
FF	fast-fast (process corners)
f_{max}	maximum oscillation frequency
f_T	unity gain frequency of a transistor’s short-circuit current gain
GaAs	Gallium-Arsenide
GCPW	grounded coplanar waveguide
GEDC	Georgia Electronic Design Center
g_m	transconductance
GPS	global positioning system
HBT	hetero-junction bipolar transistor
HCI	hot-carrier injection
HDMI	high-definition multimedia interface
HEMT	high electron mobility transistor
IC	integrated circuit
IC (org.)	industry Canada

IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IIP3	input-referred third-order-intercept point
IQ	in-phase and quadrature
J_{opt}	optimum current density
K factor	Rollet's stability factor
KVCO	VCO gain
L	inductor
LDO	low drop-out regulator
LDPC	low-density parity-check code
LNA	low-noise amplifier
LO	local oscillator
LOS	line-of-sight
LRRM	line-reflect-reflect-match calibration
LSB	lower sideband
MAC	media access control layer
MAG	maximum available gain
MIM	metal-insulator-metal (capacitor)
mmW	mm-wave, millimeter-wave
mm-wave	millimeter-wave
MOM	metal-oxide-metal (capacitor)
MOSCAP	metal-oxide-semiconductor capacitor
MOSFET	metal-oxide-semiconductor field-effect transistor
MSG	maximum stable gain
NBTI	negative bias temperature instability
NF	noise figure
NLOS	non-line-of-sight
NMOS	n-channel MOSFET
opamp	operational amplifier
P_{1dB}	1-dB gain compression point
PA	power amplifier
PDK	process design kit
PHY	physical layer
PLL	phase-locked loop
PMOS	p-channel MOSFET
PTAT	proportional-to-absolute-temperature
PVT	process, voltage, and temperature
QPSK	quadrature phase-shift keying
QVCO	quadrature voltage-controlled oscillator
RBOM	rest-of-bill-of-materials
RF	radio frequency
RFIC	radio-frequency integrated circuit
RS	Reed-Solomon error correction code
S parameter	scattering parameter
SiGe	Silicon-Germanium
SNR	signal-to-noise ratio

SoC	system-on-chip
SPI	serial peripheral interface
SS	slow-slow (process corners)
TC	temperature coefficient
TC_f	fractional temperature coefficient
TFMS	thin-film microstrip line
TT	typical-typical (process corners)
USB	upper sideband
V-band	50-75 GHz frequency band
VCO	voltage-controlled oscillator
VDD, Vdd	supply voltage
VGA	variable-gain amplifier
W-band	75-110 GHz frequency band
WiGig	wireless gigabit
WLAN	wireless local area network
WPAN	wireless personal area network
$ZTCg_m$	zero-temperature-coefficient point of transconductance

SUMMARY

With the development of wireless communication technologies, radios are evolving toward higher frequencies, wider bandwidth, and higher integration level. The millimeter-wave spectrum, especially the 60-GHz unlicensed band, presents promising potential for short-range communication. Thanks to the drastic improvement of CMOS technologies, transistors with reasonable gain at 60 GHz are available for 130-nm, 90-nm, 65-nm, and other more advanced CMOS technologies. Therefore, a millimeter-wave receiver front end can be integrated with the baseband digital and IF analog circuits on a single die, and thus achieves the goal of system on chip to reduce the production cost. Nevertheless, compared to GaAs processes, the inherent semiconductor properties of silicon substrates result in higher parasitic capacitance and loss, which also lead to the difficulty of accurate device modeling. Moreover, the process, voltage, and temperature (PVT) variations of CMOS technologies results in additional design issues different to GaAs technologies.

The objective of this dissertation is to develop key components of a CMOS heterodyne millimeter-wave receiver front end. Robust designs are necessary to overcome PVT variations as well as modeling inaccuracies, while with minimum power consumption overhead to facilitate low-power radio for portable applications. Heterodyne receiver topology is adopted because of its robust performances at millimeter-wave frequencies. Device models for both passive and active devices are developed and used in the circuit designs in this dissertation.

Two low-noise amplifiers (LNAs) are developed in this dissertation. The first LNA features a proposed temperature-compensation biasing technique, which confines the gain variation within 5 dB for temperature variation from -5 to 85 ^{o}C. The measured gain and NF are 21 and 6.5 dB, respectively, for 49-mW power dissipation. The second LNA reveals a design technique to tolerate a low-accuracy model at millimeter-wave frequencies. Both LNAs provide full coverage of the FCC 60-GHz band (57-64 GHz).

For the frequency generation circuits, both the IF QVCO and mm-wave VCO are investigated. The inherent bimodal oscillation of QVCOs is analyzed and, for the first time, a systematic measurement technique is proposed to intentionally control the oscillation mode. This technique is further utilized to extend the tuning range of the QVCO, which possesses dual tuning curves without penalty on phase noise. The measurement results of a 13-GHz QVCO in 90-nm CMOS reveals a 21.4% tuning range for continuously tuning from 11.7 to 14.5 GHz. The measured phase noise is -108 dBc/Hz at 1 MHz offset with a core power consumption of 10.8 mW. A millimeter-wave VCO is designed and fabricated in 65-nm CMOS. The VCO is fully characterized under voltage stress to examine the hot-carrier injection effects affecting the performance of a millimeter-wave VCO. The 41.6-47.4 GHz VCO is further integrated into a millimeter-wave down converter. The power-hungry buffer amplifiers are neglected by proper floor planning. Conversion loss of 1.4 dB is obtained with total power consumption of 72.5 mW.

Lastly, a power management system consisting of low-dropout (LDO) regulators is designed and integrated in a 90-nm CMOS millimeter-wave transceiver to provide stable and low-noise supply voltages. Voltage variation issues are alleviated by the LDOs.

CHAPTER 1: INTRODUCTION

1.1 Motivation

From the late 20th century to now, we have witnessed the explosive and revolutionary development of wireless communication technologies. Cellular phones allow us to talk everywhere; global positioning systems (GPS) guide us home wherever we are; wireless local area network (WLAN) connects us onto the internet over the limitation of wired cables; wireless personal area network (WPAN) further enables electronic devices to communicate, and thus becomes accessible via internet. Among these technologies, WLAN and WPAN ignite the human desire of a ubiquitous connection to the internet. It influences the cellular phone to have the same accessibility of internet because people no longer satisfy with only voice communications. People want to have data exchange and internet connections through their portable devices, which results in the popularity of 3G and 4G telecommunication standards. Nevertheless, as a consequence, the electromagnetic frequency spectrum has become overcrowded, and the demand for very high speed data links requires the availability of new frequency channels.

In 2001, the federal communication commission (FCC) released a new unlicensed band at 60 GHz with 7-GHz bandwidth extending from 57 to 64 GHz [1]-[2]. This is a turning point of radio history. It's like President Abraham Lincoln's Homestead Act enables the pioneering to the Wild West [3]. For radio-frequency (RF) engineers, millimeter-wave frequencies are our Wild West; Lots of unused broadband spectrum enables RF engineers to realize ultra-high-speed and extremely-large-capacity wireless

communication systems. Several applications are already feasible for the unlicensed 60-GHz band such as high-definition multimedia interface (HDMI) video streaming [4]. More applications, such as wireless gigabit (WiGig) high-speed communication technology, are in progress now [5]. Moreover, RF engineers are inspired to utilize the potential of other millimeter-wave frequency bands, such as E-band for mobile backhaul link [6] and W-band for mm-wave passive imager [7]. We can assert that the next wireless wave is a millimeter-wave [8].

Although mm-wave communication seems to have a promising future, the required millimeter-wave radio-frequency (RF) front end may become a show stopper for cost consideration. In the past, millimeter-wave (mm-wave) front-end circuits are dominated by GaAs-based high electron mobility transistor (HEMT) and hetero-junction bipolar transistor (HBT) processes because of the superior high frequency characteristics of the device and the high quality passive components on the semi-insulating substrate. However, GaAs technologies are unable to be integrated with complementary metal-oxide-semiconductor (CMOS) base-band circuits. Higher cost for additional package obstructs the expansion of GaAs technology applications from military to civil purposes. On the contrary, CMOS technologies are preferred to mm-wave front-end circuits because of their cost and ease of integration. Fortunately, with the rapid evolution of CMOS technologies, current CMOS technologies are able to provide enough operation speed for mm-wave front-end circuits. For example, a cost effective 130-nm standard digital CMOS process has a unity gain frequency of 90 GHz. The current mainstream technologies for radio system-on-chip (SoC) are 90- and 65-nm CMOS, which reveal unity gain frequency of a transistor's short circuit current gain (f_T) of 160 and 200 GHz,

respectively. Therefore, recent publications have demonstrated the feasibility of implementing mm-wave transceivers in 0.13-μm [9], 90-nm [10]-[12], 65-nm [13], and other more advanced CMOS technologies. These publications claim that the CMOS mm-wave transceivers are now achieving reasonable performance for indoor short-range link applications, but with much higher integration level and also lower cost when compared to GaAs-based transceivers.

However, there are still some obstacles for evolving the 60-GHz CMOS radio from a research prototype to a manufacturable product. These problems are originated from the basic material property of silicon. Although transistors that are able to operate at mm-wave range are now available in CMOS technologies, the lossy nature of the silicon substrate makes CMOS mm-wave front-end designs challenging. The higher loss with increasing operating frequency leads to poor quality factors of the on-chip passive components. Because of the lossy silicon substrate, more parasitic effects are introduced by the substrate leakage current compared with GaAs processes. These parasitic effects lead to inaccuracy of the RF model for both transistors and passive components. Moreover, classic problems of process, voltage, and temperature (PVT) variations inherent to CMOS technology become more severe at mm-wave frequency.

1.2 Challenges

1.2.1 **Modeling Inaccuracy**

Most of current successful mm-wave transceiver designs were not done with a single tape out. The mainstream design flow of the mm-wave transceiver is usually divided into three steps: (1) a test structure tape out for characterizing the mm-wave model of both passive and active components [14], (2) an individual block tape out

including all the mm-wave amplifiers, mixers, and voltage-controlled oscillators (VCOs) [15], and (3) a full transceiver tape-out [11]. The first-pass design flow, which is usually applied for fully integrated RF transceiver below 10 GHz [16], cannot be directly transplanted to mm-wave frequencies because of the lack of accurate models. Nevertheless, the conservative three-step mm-wave design flow not only increases the cost, but it also increases the development time. Cost and time to market are the most important two factors for a successful project in current competitive integrated circuit (IC) industry. Therefore, obviously, the aforementioned conservative mm-wave IC design flow is not favored for the current SoC market evolution trend.

The essential problem causes the aforementioned issues is: "Why the available foundry-provided models may be not good enough for mm-wave front-end IC designs?" To answer this question, let's take two major functional blocks in a receiver front end, the amplification circuit and the signal generation circuit, as examples to elaborate the deviations in the required accuracy levels of the device models for multi-GHz RFICs (below 10 GHz) and for mm-wave front-end ICs.

A voltage-controlled oscillator (VCO) as shown in is taken as our first example. The oscillation frequency is given by the equation:

$$f = \frac{1}{2\pi\sqrt{LC}}, \tag{1.1}$$

where L and C are the inductance and the capacitance of the resonator. For mm-wave VCO, the required L is around several hundreds of pico-Henry and C is around several tens of fento-Farads. For example, a 60 GHz VCO can use a combination of an inductor

of 250 pH and a varactor of 28 fF. The small inductance and capacitance values increase the difficulty of modeling. Furthermore, the parasitic capacitance of the transistor affects significantly of the oscillation frequency, but the parasitic capacitances are usually difficulty to be predicted accurately, especially for the layout-induced parasitic capacitances.

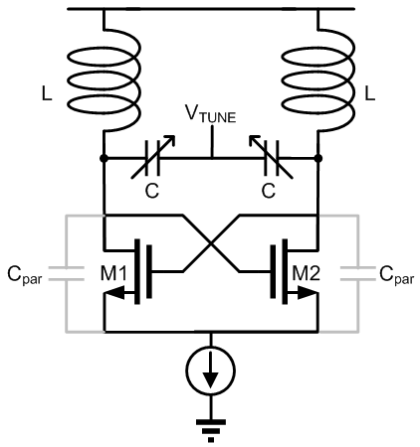


Figure 1.1. Conceptual schematic diagram of a voltage-controlled oscillator (VCO).

Secondly, let us focus on the mm-wave signal amplification circuit. In a receiver front end, the low-noise amplifier (LNA), serving as the first amplification circuit that amplifies the weak RF signal received by the antenna while minimally degrading the signal-to-noise ratio (SNR), has to be operated at the highest frequency of a mm-wave receiver. Therefore, it is unavoidable that we need to deal with the cumbersome parasitic elements, which may significantly affect the band-pass response of the LNA, at millimeter-wave frequencies. Moreover, the maximum available gain (MAG), which will be depicted in Section 4.1.2.3, rolls off dramatically with the increase of frequency. Therefore, to obtain the required gain, cascading of multiple gain stages is necessary. As

a consequence, the RF performance impairments, which are caused by an erroneous prediction of inaccurate models, become more severe.

Since signal amplification and frequency generation are the most critical functional blocks in a receiver front end, in this dissertation, methods will be proposed for designing operable LNAs and VCOs against modeling uncertainties. Inaccurate modeling may cause additional problems for different building blocks in a receiver front end, such as potential oscillation for an mm-wave LNA or bimodal oscillation for an intermediate-frequency (IF) quadrature voltage-controlled oscillator (QVCO). These are also critical issues and practical solutions are proposed and verified in this dissertation as well.

1.2.2 **PVT Variation**

PVT variations, which are inherited to CMOS technologies, are classic problems that troubled analog designers for decades. As CMOS technologies move forward to deep sub-micron and nanometer nodes, the sensitivity of circuits towards PVT variations increasingly degrades the RF and analog circuit performances, making the design of sensitive analog/RF circuits in these technologies extremely difficult. To deal with the PVT variations, analog designers developed circuit techniques to reduce the performance degradation caused by PVT variations. These techniques include special considerations on biasing circuitry (e.g., constant trans-conductance (g_m) bias [17]), on temperature compensation (e.g., bandgap reference voltage circuit [18]), and on the layout optimization (e.g., common-centroid layout [19]). At mm-wave frequencies, the PVT variation effects become more severe because of two major reasons: (1) mm-wave circuits are more sensitive to parasitic capacitance, resistance, and inductance. These

parasitic elements are varied significantly because of PVT variations. (2) mm-wave circuits are usually tuned circuits, which use inductors to tune out the parasitic capacitances for band-pass responses. The PVT variations, which only cause a bandwidth reduction in low-pass analog/RF circuits, may cause a drastic frequency shift for band-pass mm-wave circuit, thus result in a failure of the system. To deal with the PVT variations for mm-wave circuit, although some of the aforementioned techniques can be directly applied in mm-wave designs to alleviate the PVT variation effects, most of the low-frequency analog techniques need to be revised for mm-wave circuit designs. Current publications of mm-wave transceivers rarely mentioned about the performance degradation caused by PVT variations. It is not because that PVT variations cause negligible effects on mm-wave circuits. On the contrary, PVT variations cause significant effects on the uniformity of CMOS mm-wave circuit performances. The variation of the circuit performances become an obstacle for mass production of CMOS mm-wave transceivers.

Process variation usually presents as process corners. The four extreme corners are fast n-channel MOSFET (NMOS) and fast p-channel MOSFET (PMOS), slow NMOS and slow PMOS, fast NMOS and slow PMOS, and slow PMOS and fast NMOS, respectively. The corner is specified due to the actual variation of the process, usually marked as 3-sigma variation. Temperature dependent models for MOSFETs are also provided along with the process design kit (PDK). Therefore, circuit performances under reasonable variation range for process, voltage, and temperature can be simulated. Specification needs to be satisfied for these process corners to ensure reasonable yield. Conventional approach is to over design toward some sensitive design specifications.

However, over design usually means trade off on other specifications, such as higher power consumption or larger chip area.

Currently, the concept of self healing or self calibration is proposed to overcome the PVT variations in low frequency RF building blocks [20]-[21]. Nevertheless, the self-healing/calibration techniques require sensors and analog-to-digital converters (ADCs). Operating at mm-wave frequency, sensors and ADCs are not feasible for current CMOS technology. An alternative solution for the PVT variations in the proposed research is to perform sensitivity analysis of the key components in an mm-wave receiver. Proper design of the building blocks can make the performance less sensitive to the variations. This is the basic design guideline for the all the mm-wave front-end components in the research proposal. In addition, regulators are designed to provide a stable voltage with less variation for supply voltage of the mm-wave circuits. Temperature compensated current biasing technique mitigates the temperature variation effects. The design of these supply regulation and biasing blocks are essential parts of this dissertation as well.

1.3 Organization of Dissertation

The dissertation is organized as follows. Starting with the research objective and challenges in chapter 1, chapter 2 provides an overview of the millimeter-wave receiver front end. This research emphasizes on the 60-GHz band. Therefore, chapter 2 introduces channel characteristics and current regulation and standardization efforts of this band. The performance trade-offs between wireless receivers architectures are analyzed as well. After a summary of the state-of-the-art silicon mm-wave receiver front end, receiver front end architecture is determined and design specifications are calculated by a brief link budget analysis for the critical building blocks.

Chapter 3 introduces the device modeling for millimeter-wave receiver front end design. This chapter is divided into passive components modeling and active devices modeling. Since a foundry provided model is available for the CMOS technology used here, this chapter does not provide modeling methods from scratch device measurement. However, this chapter emphasizes on the improvement of the existing model for a feasible mm-wave design. Moreover, for some components that usually lack of foundry-provided models, such as transmission lines for microwave designs, a step-by-step modeling procedure is elaborated in this chapter.

After the device models for mm-wave frequencies have been established, the dissertation continues to discuss the circuit design techniques to overcome the aforementioned two major obstacles, modeling inaccuracy and PVT variations, for successful mm-wave receiver front end designs. Critical building blocks, as illustrated in Figure 1.2, are designed and analyzed in the following chapters.

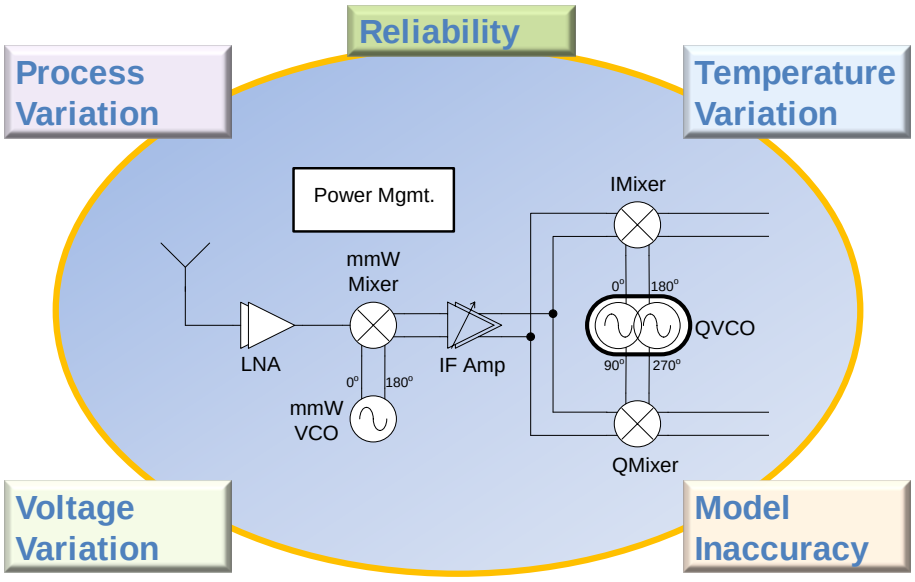


Figure 1.2. Critical building blocks and design challenges of an mm-wave receiver front end.

Chapter 4 introduces the design of mm-wave low-noise amplifier (LNA). Based on the fundamentals depicted firstly in this chapter, two LNA design methodologies are introduced as treatments of modeling uncertainty and temperature variation. The LNAs reveal gain larger than 20 dB and wide 3-dB bandwidth covering the entire 57-64 GHz usable spectrum. Under temperature variation from -5 to 85 ^{o}C, the measured LNA gain is confined within 5 dB variation.

Frequency generation circuits are presented in Chapter 5. The 13-GHz IF QVCO is analyzed firstly with focus on the inherent bimodal oscillation phenomenon. A systematic measurement technique is proposed and verified to control the QVCO oscillation mode. Moreover, this phenomenon is utilized to extend the frequency tuning range to 21.4% by controlling the predictable dual-oscillation modes. Second part of this chapter investigates the reliability issues of mm-wave VCO under voltage stress. A complete characterization on an mm-wave cross-coupled VCO is performed to quantify the performance degradations caused by hot-carrier injection (HCI) effects. In the last part of this chapter, this mm-wave VCO is integrated into an mm-wave down converter.

In order to handle the voltage variation induced performance degradation of mm-wave receiver front ends, power management system is designed and analyzed in Chapter 6 to provide a stable and clean supply voltage. The low drop-out regulator (LDO) designed in this chapter is able to provide 1 and 1.2 V output voltages. It supports maximum output current of 200 mA while draws a quiescent current of 620 μA.

The contributions of this research work are summarized in the final chapter. Potential future research opportunities are also discussed in the end.

CHAPTER 2: MILLIMETER-WAVE RECEIVER FRONT END OVERVIEW

2.1 Introduction to Communication in the 60-GHz Band

2.1.1 Regulations and standardization of the 60-GHz band

In January 23rd, 2001, FCC realigned the 50.2-71 GHz spectrum and therefore released the band between 57-GHz and 64-GHz for unlicensed uses [1]-[2]. The average power density is regulated to 9 $\mu W/cm^2$, which equals to 40 dBm equivalent isotropically radiated power (EIRP). The maximally allowed peak power density is twice of the average power density, which is 43 dBm EIRP. Canadian 60-GHz regulations, issued by the Industry Canada (IC), mostly conform to the US FCC. However, the lower band (57-59GHz) is not fully released and is reserved to augment the existing unlicensed band (59-64 GHz).

In Europe, the 57-66 GHz frequency band is allocated for unlicensed use all over the European Union by the regulations harmonized by the European Telecommunication Standards Institute (ETSI) [22]. The indoor power density limit is 13 dBm/MHz EIRP with a maximum total power level of 40 dBm EIRP. For devices used both indoor and outdoor, EIRP is maximally 25 dBm, which is 15 dB less than the indoor limit.

In Japan, the band between 59- GHz and 66-GHz is allocated for unlicensed use. The maximum transmitter power is limited to 10 mW (10 dBm) and the maximum antenna gain is 47 dBi, which gives a maximum EIRP of 57 dBm [23].

Other countries also released spectrum around 60-GHz for unlicensed applications as shown in Figure 2.1. As a result, at least 3.5-GHz unlicensed bandwidth

around 60-GHz is available worldwide. The broad bandwidth, as well as license-free convenience, makes 60-GHz band very attractive for high data rate consumer electronic applications.

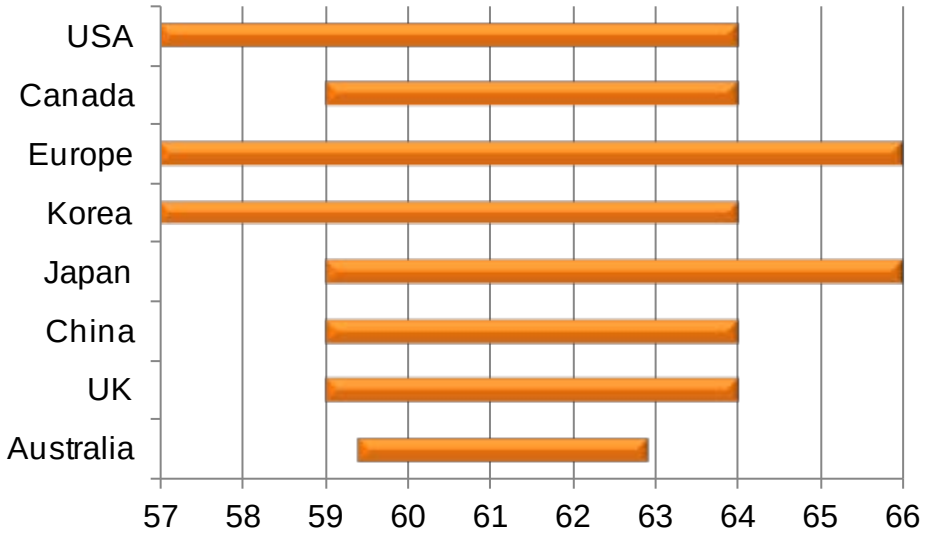


Figure 2.1. Summary of the worldwide unlicensed band around 60 GHz.

To exploit the broadband potential of 60 GHz, numerous standards are proposed for high-speed data transfer, high-definition video streaming, next generation Wi-Fi networks, and other emerging applications. With the effort of several organizations (i.e., IEEE 802.15.3c [24], IEEE 802.11.ad [25], ECMA 387 [26]), communication standards using the unlicensed 60-GHz band are rapidly converging. IEEE 802.15.3c is the first standard for 60-GHz band. To compromise the inconsistency of spectrum allocation at different countries, IEEE 802.15.3c divides the full 60-GHz band into 4 channels as shown in Figure 2.2 [24]. The carrier frequencies of neighboring channels are separated by 2.16 GHz. Only a part of these channels are used depending upon the regional spectrum allocation. Other standards are inspired by IEEE 802.15.3c and therefore adopt

the same channel frequency separation planning. IEEE 802.15.3c, IEEE 802.11.ad, and ECMA 387 standards define the physical layer (PHY) and media access control layer (MAC) in the seven-layer open system interconnection (OSI) model of computer networking.

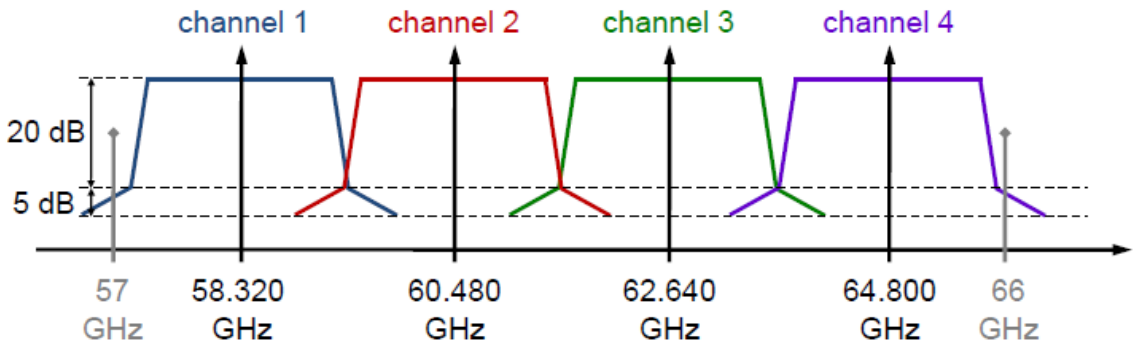


Figure 2.2. Band division for 4 channels defined by the IEEE 802.15.3c [24].

In addition to IEEE 802.15.3c, IEEE 802.11.ad, and ECMA 387, WirelessHD [4], [27] and WiGig [5] are the other two specifications that are more familiar to end-users. The WirelessHD standard is dedicated for deliver high definition, uncompressed video/audio contents. In WirelessHD ver. 1.0a, it supports uncompressed 1080 pixel resolution (1080p) with data rates up to 4 Gb/s. In the newest version 1.1d1, it is able to support 2160p, which is called “Quad HD”, with data rates up to 7.1 Gb/s. However, the WirelessHD is more like a point-to-point proprietary link therefore the introduction will stop here without mentioning its detailed technical specifications.

WiGig specification is oriented for data transmission in the context of Wi-Fi networks. It defines PHY and MAC layers. The WiGig specification features backward compatibility to current IEEE 802.11 standards. Thus, WiGig specification was contributed to the IEEE 802.11ad standardization process, and was confirmed in May 2010 as the basis of the 802.11ad draft standard. In summary, the core technologies standards of 60-GHz frequency band are tabulated in Table 2.1. WirelessHD and WiGig are not included in this table because of the aforementioned reasons: WirelessHD is proprietary point-to-point link standard for the consortium participants and WiGig serves as a basis for the emerging 802.11ad standard.

Table 2.1: Wireless communication standards utilizing the 57-66 GHz band.

Standard	802.15.3c		802.11ad		ECMA 387	
PHY Type	Single-carrier	OFDM	Single-carrier	OFDM	Single-carrier	OFDM
Modulation Constellation	BPSK, GMSK, QPSK, 8PSK, 16QAM	QPSK, 16QAM, 64QAM	π/2-BPSK, π/2-QPSK, π/2-16QAM	OQPSK, QPSK, 16QAM, 64QAM	BPSK, QPSK, NS8QAM, 16QAM	QPSK, 16QAM
Data Rate [Mbps]	25.3-5100	31.5-5670	385-4620	693-6756	397-6350	1008-4032
Coding*	RS, LDPC	LDPC	LDPC	LDPC	RS, CC	RS, CC
BW [GHz]	1.782		1.88		1.728	
Center Frequency [GHz]	CH1: 58.32, CH2: 60.48, CH3: 62.64, CH4: 64.80					

*The abbreviation of each different coding is listed below:

RS: Reed-Solomon error correction code; LDPC: Low-density parity-check code; CC: Convolutional Code.

2.1.2 **Characteristics of the 60-GHz band**

Before introducing the channel characteristic of the 60-GHz band, we have to acknowledge that the high path loss nature of this specific band. Because of the high path loss of 60-GHz band, FCC allows a high average transmit power (40 dBm EIRP) to overcome the channel characteristic as mentioned in the previous section. The lossy channel is mainly due to the free-space loss and the oxygen absorption.

The free-space line-of-sight (LOS) path loss can be characterized by the Friis transmission formula given by [28]:

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi R} \right)^2 , \tag{2.1}$$

where P_r and P_t are the received and transmitted power in mW, G_t and G_r are gains for the transmit and receive antenna, R is the distance between the two antennas in meters, and λ is the signal wavelength in meters. From the Friis formula, the signal attenuation can be viewed as a multiplication of three terms: the transmit antenna gain, the receive antenna gain, and the path loss. It is obvious that path loss is inverse proportional to the square of distance, and proportional to the square of wavelength. Since wavelength is inverse proportional to the frequency, the path loss is inverse proportional to the square of frequency as well. For an arbitrary distance, the path loss at 60 GHz is 625 times larger than the loss at 2.4 GHz, which equals to an additional 28 dB loss. This implies a much shorter transmission distance for 60-GHz communication within a limited power budget. Although the antenna possesses higher gain for a relatively smaller area, however, at 60 GHz even an antenna having a small effective area is very directive. The increment in

antenna gain can only mitigate the path loss, but cannot fully compensate. Furthermore, extra efforts have to be spent on techniques increasing the beam width and the receiving angle (e.g. beam forming [4]).

In addition to the high path loss at all millimeter-wave frequencies, 60-GHz band attributes higher loss comparing to other mm-wave bands to oxygen absorption [29]. The presence of atmospheric gases such as oxygen and water vapor further attenuates the signal. This can be seen as a peak of the sea level attenuation in the left plot of Figure 2.3. Moreover, rain attenuation further degrades the loss at mm-wave frequencies. From the Figure 2.3, it is found that the rain attenuation increases proportional to the frequency in a log-log scale and saturates at mm-wave frequencies.

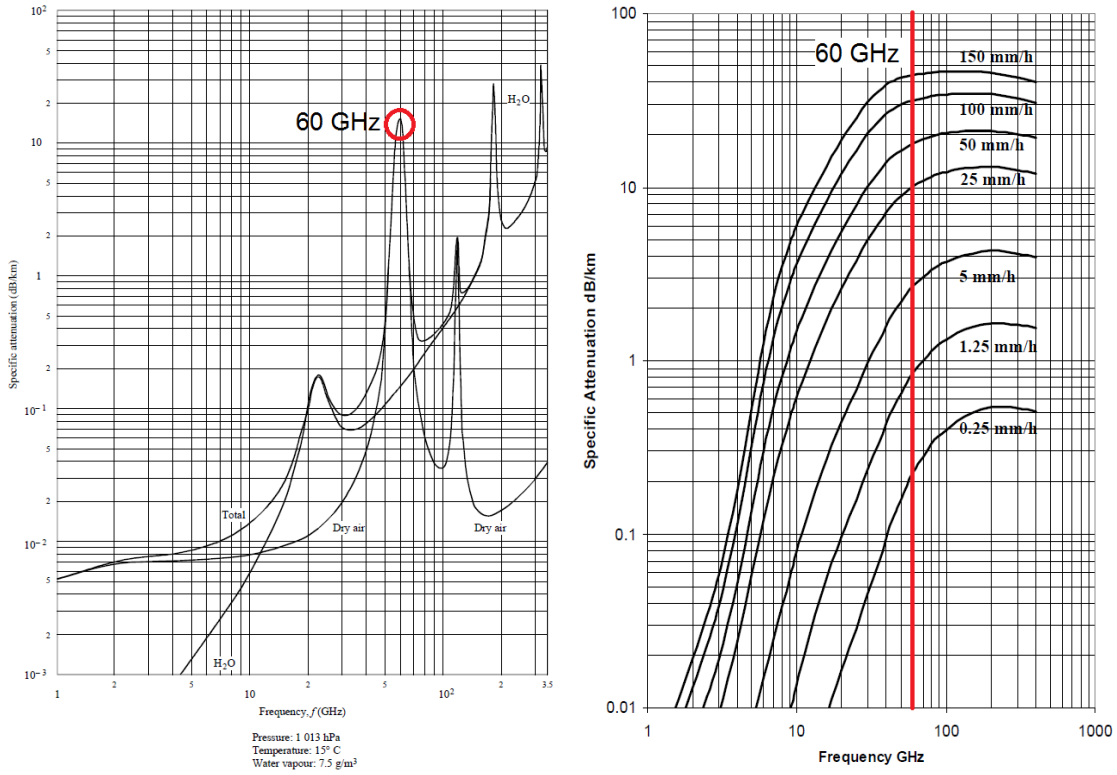


Figure 2.3. Sea level attenuation (left) and rain attenuation (right) [29]-[30].

The lossy nature of 60-GHz channel results in some unique attributes. Although the range of communication is therefore limited, this phenomenon provides advantages on interference and security. For indoor short-range communication, the 60-GHz signal rarely leaks out of the building, which guarantees the channel is almost impossible to eavesdrop and the in-band interference is negligible. Furthermore, this is a great advantage in terms of frequency reuse.

Table 2.2 summarizes the channel characteristics of two unlicensed bands: 2.4-GHz band and 60-GHz band. The unique properties make 60-GHz band a promising candidate for ultra-high speed indoor communication.

Table 2.2. Channel characteristic comparison between 2.4-GHz band and 60-GHz band.

Specification	2.4 GHz	60 GHz
Bandwidth	Narrow	Large
Path Loss	Low	High
Antenna Effective Area	Large	Small
Antenna Pattern	Omni-directional	Narrow Beam
Interference	Complicated	Negligible
Frequency Reuse	Hard	Easy
Security	Moderate	Good

2.2 Receiver Architectures

The simplest form of receiver is a non-coherent detector, which detects the envelope of the modulated RF signal without extracting the carrier frequency. Millimeter-wave receiver exploiting non-coherent detection features low-power, low-complexity, and low-cost [31]. However, comparing to coherent receivers, non-coherent receiver suffers from an inferior sensitivity because of the lack of a high precision and low-noise signal template. Moreover, only amplitude-modulated information can be detected by the non-coherent receiver, prohibiting the use in phase or frequency-modulated signal demodulators.

Coherent detection multiplies the carrier frequency to the received RF signal, thereby down converting the RF signal to the baseband (BB). Depending on the down conversion is done in a single step or in two steps, coherent receiver can be distinguished into direct-conversion receiver, which directly down converts the RF signal to BB, and heterodyne receiver, which inserts an intermediate frequency (IF) as a relay between RF to BB.

2.2.1 **Direct-conversion receiver**

Direct-conversion receiver, also called as homodyne receiver or zero-IF receiver, is illustrated in Figure 2.4. The RF signal received by the antenna, after amplified by the LNA, is multiplied by the LO signal having the same frequency as the RF carrier. Both the upper sideband (USB) and lower sideband (LSB) spectra down convert to the baseband and overlap with each other. If USB and LSB do not carry the modulated signal from the same BB, the mixing results in an incomprehensible output. The quadrature mixing shown in Figure 2.4 solves this issue. The information carried by USB and LSB

can be demodulated by I and Q paths separated by LO signals with 90 degree phase difference even though different information are carried by USB and LSB.

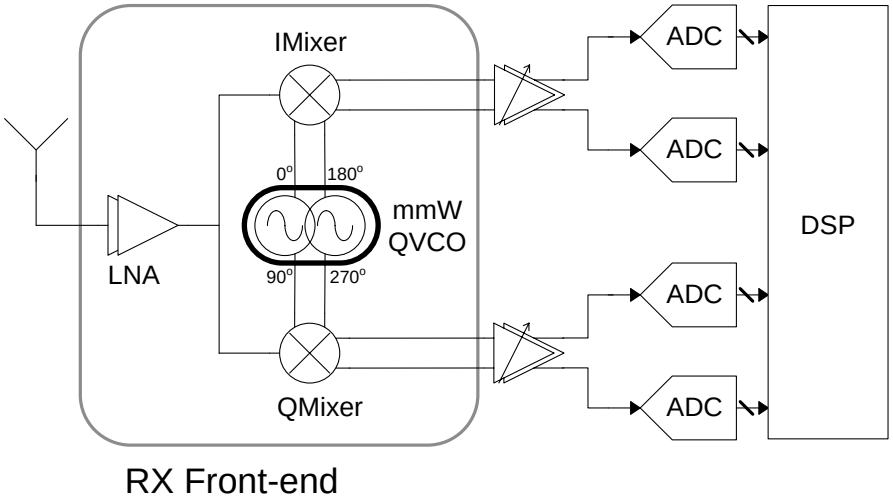


Figure 2.4. Direct-conversion receiver block diagram.

Comparing to heterodyne receivers introduced in next section, direct-conversion receiver requires less components. This implies that direct-conversion receiver dissipates less power and is more suitable for monolithic integration. Nevertheless, major issues such as dc offset, I/Q mismatch, even-order distortion, LO leakage, and flicker noise limit the performances of direct-conversion receiver, which have been investigated by the pioneers in the early ages of CMOS RF [32]. Nowadays, most critical issues are solved. Although heterodyne receivers still possess superior sensitivity, thanks to the digital calibration and signal processing techniques, performance gap between direct-conversion and heterodyne receivers have reduced tremendously. Currently, CMOS direct-conversion receiver becomes the mainstream for low-frequency radio architectures.

2.2.2 **Heterodyne receiver**

Heterodyne receiver, as illustrated in Figure 2.5, down converts the RF signal received by the antenna twice to the BB with IF serving as a relay. Heterodyne receivers have been presented for a long time, and provide the highest fidelity to accommodate various applications. The RF signal received by the antenna is first amplified by the LNA. According to the band-pass frequency response of the mmW LNA, it offers the function of interference filtering by properly selection of the RF bandwidth and out-of-band attenuation. The amplified RF signal is then multiplied by a mmW local oscillator (LO) signal represented by $A_{LO}cos(\omega_{LO}t)$. As a consequence, the output of the mixer lies in two bands, one is around ω_{RF}-ω_{LO}, and another is around ω_{RF}+ω_{LO}. The high frequency component is filtered out and therefore down converts the RF signal into the IF band, where ω_{IF}=ω_{RF}-ω_{LO}. In Figure 2.5 the filter function is provided by the LC-tuned load response of the mixer and additional attenuation provided by the frequency response of the band-pass IF VGA. The second down conversion from IF to BB is performed in a similar manner as a direct-conversion down converter. As explained in Section 2.2.1, I/Q demodulation is required to preserve information loaded on USB and LSB. Although the second down conversion functions as direct-conversion receiver, the specifications of the second down conversion are quite relaxed comparing to a direct-conversion receiver. The second down conversion only needs to accommodate a relatively smaller dynamic range because of the function of IF VGA. Moreover, interferences are already filtered out by the front-end circuits therefore the second down conversion is operated in a simpler environment. This also alleviates the critical issues for direct-conversion receivers, such

as dc offset, I/Q mismatch, even-order distortion, LO leakage, and flicker noise, in heterodyne receiver topologies.

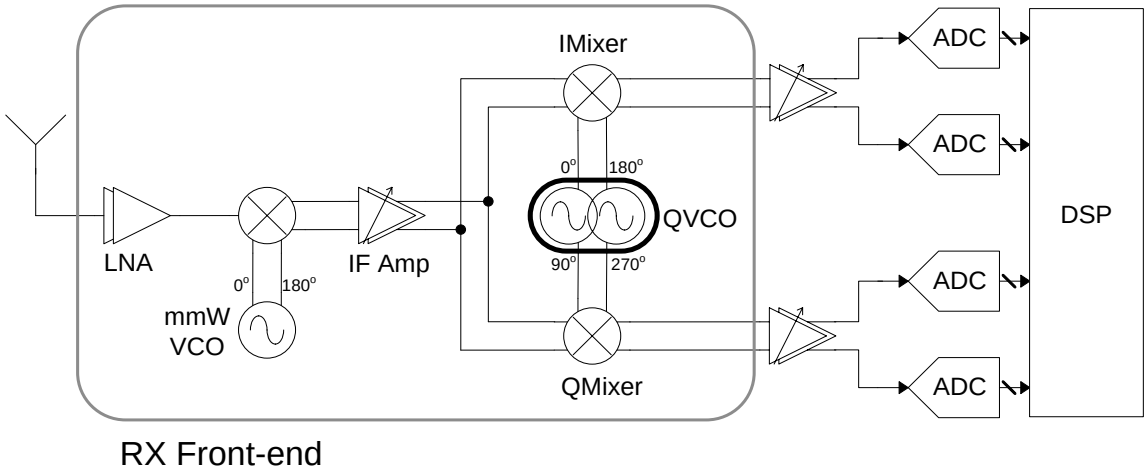


Figure 2.5. Heterodyne receiver block diagram.

A serious problem of heterodyne receiver is image frequency. As shown in Figure 2.6, not only the desired RF signal ($\omega_{RF}=\omega_{LO}+\omega_{IF}$) but also the unwanted "image-frequency" interference lies at $\omega_{IM}=\omega_{LO}-\omega_{IF}$ fold into the IF band after down conversion. If a strong interference appears at ω_{IM}, the IF signal becomes distorted. One common solution is to place an image-rejection filter at the RF input. However, a high-quality filter is difficult to be implemented on-chip by the passive components on a lossy silicon substrate, yet an off-chip solution increases cost and form factor. As a result, it is preferred to utilize the frequency response of the LNA to achieve the desired attenuation at ω_{IM}. Since $\omega_{IM}=\omega_{LO}-\omega_{IF}$ and $\omega_{IF}=\omega_{RF}-\omega_{LO}$, the selection of the LO frequency significantly determines the performance of a heterodyne receiver and will be discussed in the next paragraph.

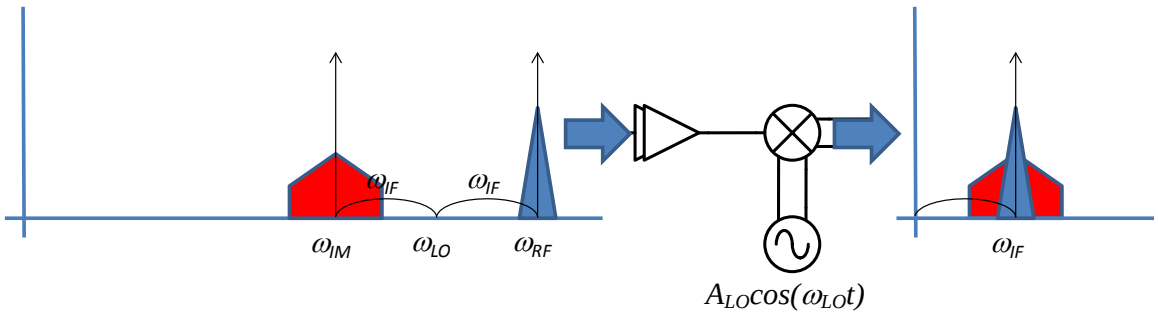


Figure 2.6. Problem of image frequency in a heterodyne receiver.

The selection of the intermediate frequency is a tradeoff between image rejection and channel selectivity as depicted in Figure 2.7. The higher the IF is selected, the better the image can be attenuated by a given filter as the separation of the signal to the image interference getting larger. However, when it is down converted to the IF band, the channel select filter, which has a center frequency at ω_{IF}, attenuates the adjacent channel interferers depending on the IF selection as well. For channel select filters with the same quality factor (i.e. same fractional bandwidth), the higher the frequencies are, the larger the absolute bandwidths are. Therefore, a high IF yields to lower adjacent channel interferer suppression. As a result, high IF yields a good image rejection, but a worse channel selectivity. On the other hand, low IF suffers from a worse image rejection, but can suppress the adjacent channel interferer better.

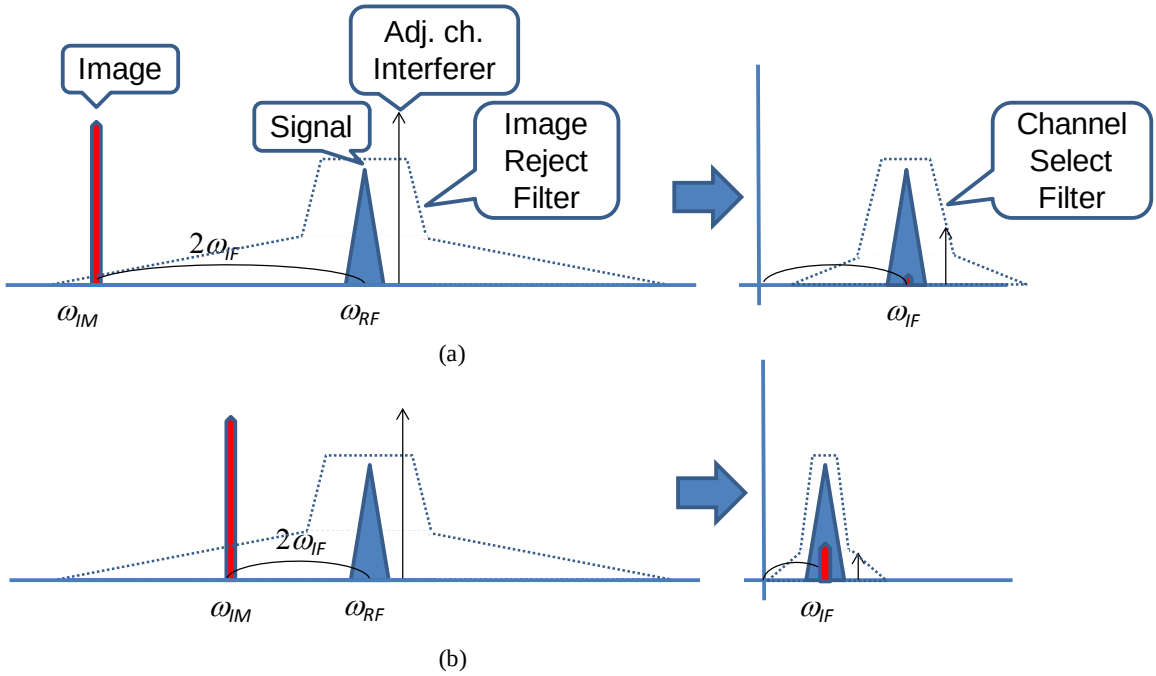


Figure 2.7. Rejection of image versus suppression of adjacent channel interferers for (a) high IF and (b) low IF.

2.2.3 State-of-the-art 60-GHz Si-based receiver front end

Since the 60-GHz band was released in 2001 by FCC, researchers all over the world started to attempt various approaches to realize low-cost and high-performance 60-GHz radio. Receiver front ends play an important role in the radio, and therefore draw lots of attention for research and development. Since silicon-based processes are proved as best candidate in terms of cost and integration level, researches in this specific area mostly adopt CMOS and SiGe BiCMOS as the platform to develop their radios. In this section, the state-of-the-art 60-GHz receiver front ends developed by various research groups globally are reviewed and summarized, where the majority of them are developed in CMOS technologies and the rest are developed in SiGe owing to superior RF performances.

Non-coherent detector, because of simplicity and low-power consumption, is developed by numerous research groups as their first step of millimeter-wave RF front-end development. Dr. Laskar's research group in Georgia Tech used a diode as a square-law detector in SiGe [33], and then developed a modified version using self-mixer in CMOS [31]. J. Lee's research group in National Taiwan University developed a receiver that first down convert the 60-GHz signal to a lower IF frequency, then use an envelope detector for non-coherent demodulation [10]. Research group of Sony proposed a hybrid solution, between non-coherent and coherent detection, to improve the sensitivity [34]: the 60-GHz RF signal is first down converted by a LO, which is injection locked by the RF signal, and then the down-converted signal is demodulated by envelope detector. These non-coherent detectors feature very low-power, low-cost, and low-complexity implementations without the need of a precise reference LO with appropriate phase. But the limitations of low sensitivity, short distance, and low flexibility to modulation schemes restrict their applications.

Direct-conversion topology is a popular choice for 60-GHz receiver front ends in published literatures. The first 60-GHz receiver was developed by IBM in SiGe and direct-conversion topology was adopted [35]. The first CMOS 60-GHz receiver front end used direct-conversion topology as well, which is developed by B. Razavi of UCLA in 2005 [36]. Other successful 60-GHz direct-conversion receiver demonstrations are from J. Tsai of National Taiwan Normal University [9], S. Voinigescu's research group in University of Toronto [13], T. Mitomo et al. of Toshiba [37], and M. Tanomura et al. of NEC [38]. The highest level of integration reported so far for 60-GHz direct-conversion

receiver originated from University of California, Berkeley [11] and Tokyo Institute of Technology [39], both of them demonstrated a complete transceiver in one die.

Heterodyne receivers feature superior RF performances in terms of sensitivity. Because of the high free-space path loss at 60 GHz, improvement of sensitivity becomes precious for better communication range. The first CMOS heterodyne receiver front end was presented by S. Emami et al. from University of California, Berkeley in 2007 [40]. This successful receiver front end later became a basis of their start-up company, SiBeam, which developed phased-array transceivers for WirelessHD and eventually was acquired by SiliconImage [4]. In UCLA, B. Razavi's research group proposed a heterodyne receiver [41] and later the same research group developed another 60-GHz CMOS heterodyne receiver using 30-GHz LO for both first and second down conversion [12]. Here in Georgia Tech, heterodyne receiver with fixed IF topology was developed [42]. Fixed IF topology only changes the LO frequency while fixes the IF, therefore keeps the center frequency and bandwidth of the IF circuits remain constant to facilitate the system design. On the other hand, IBM adopts "sliding IF" frequency plan where both LO and IF change while band switching [43]. Sliding IF keeps the frequency ratio of LO and IF to be a constant, therefore both LO and IF can be generated by a single oscillator with frequency multiplier or divider to save power consumption.

It is worth mention that, interestingly, some research groups started with direct-conversion architecture eventually switched to heterodyne. Examples can be found in IBM ([35] and [43]), Toshiba ([37] and [44]), and Razavi's group of UCLA ([36] and [41]). It is presumed that the architecture is changed for the pursuit of better performances. Moreover, the only available off-the-shelf silicon 60-GHz receiver IC,

HMC6001 provided by Hittite Microwave Corporation, also adopts heterodyne architecture [45]. HMC6001 is a SiGe fully integrated mm-wave receiver IC. Currently, there is still no CMOS mm-wave receiver IC product available in the market. All these state-of-the-art 60-GHz silicon receiver front ends are summarized in Table 2.3.

Table 2.3. Performance summary of state-of-the-art 60-GHz silicon receiver front ends.

Ref./Tech.	Architec-ture	Integration						Freq. (GHz)	NF (dB)	Gain (dB)	Power Con-sumption (mW)
		Antenna	LNA	Mixer	VCO	PLL	VGA				
[33] 0.18-μm SiGe	Non-coherent detection	✓ (Patch)	✓					58-63	7.9	24	25
[31] 90nm CMOS	Non-coherent detection		✓	✓ (Self-mixer)				60	8.5	N/A	108
[10] 90nm CMOS	Down conversion + Non-coherent detection	✓ (Patch)	✓	✓	✓			60	7.3	24.8	103
[34] 40nm CMOS	Injection-locking LO + ASK	✓ (Bond wire)	✓	✓	✓			56	8	20	41
[35] 0.12-μm SiGe	Direct-conversion		✓	✓				61.5	5-6	33	313
[36] 0.13-μm CMOS	Direct-conversion		✓	✓				60	12.5	28	9
[9] 0.13-μm CMOS	Direct-conversion		✓	✓				55-64	10.2	7.2	90
[13] 65nm CMOS	Direct-conversion	✓ (Horn)	✓	✓				60	5.6	14.7	151
[37] 90nm CMOS	Direct-conversion		✓	✓	✓	✓	✓	61.34 -63.4	8.4	21.8-22.5	144

Table 2.3. Continued.

[38] 90nm CMOS	Direct-conversion		✓	✓			✓	62	8.4 (LNA only)	18.7 (LNA) & -4 to 14 (VGA)	206
[11] 90nm CMOS	Direct-conversion	✓ (Horn)	✓	✓	✓	✓	✓	60	N/A	N/A	138
[39] 65nm CMOS	Direct-conversion	✓ (Patch)	✓	✓	✓	✓	✓	51-68	<8	4.7 to 17.3 (Adjust-able)	106
[40] 0.13-µm CMOS	Hetero-dyne, Fixed IF		✓	✓	✓			60	10.4	11.8	76.8
[41] 90nm CMOS	Hetero-dyne, Sliding IF		✓	✓	✓			49-53	6.9-8.3	26-31.5	80
[12] 90nm CMOS	Hetero-dyne, Single 30-GHz LO		✓	✓	✓			60	5.7-8.8	18.3-22	36
[42] 90nm CMOS	Hetero-dyne, Fixed IF	✓ (Patch)	✓	✓	✓	✓	✓	57-66	8	32	189
[43] 0.13-µm SiGe	Hetero-dyne, Sliding IF	✓ (Planar)	✓	✓	✓	✓	✓	59-64	5-6.7	38-40	526.5
[44] 65nm CMOS	Hetero-dyne, Sliding IF	✓ (Bond wire)	✓	✓	✓	✓	✓	57-66	14	35	233
[45] SiGe	Hetero-dyne, Sliding IF	✓	✓	✓	✓	✓	✓	57-64	6	2 to 65 (Adjust-able)	610

2.2.4 **Adopted receiver architecture**

Direct-conversion receiver featuring low complexity and low power has become the mainstream receiver architecture for low-frequency-band communications. In the

development of CMOS mm-wave receiver, some researchers attempt to keep these advantages at a much higher frequency. On the other hand, some researchers decide to embrace the heterodyne architecture because of unique features that only heterodyne receivers can offer. In this section, both architectures will be analyzed in order to minimize the performance degradation caused by modeling inaccuracy and PVT variation. Suitable receiver architecture will be determined as a first step for a successful first-pass receiver front end design.

Direct-conversion receiver, if all the features at low frequency can be directly applied at mm-wave frequencies, is the first choice for most of the RF system architect. Nevertheless, three bottlenecks are found inherently to the direct-conversion receiver, and deteriorate the RF performance as frequency goes higher. Firstly, for IQ demodulation, an mm-wave quadrature frequency source and mixing component are required in a direct-conversion receiver. However, even slight device mismatch or unequal routing may cause significant in-phase and quadrature (IQ) mismatch at such a high frequency. Phase calibration techniques have been developed for low frequency. Unfortunately, it is still not applicable for mm-wave frequencies.

Secondly, since the IF stage is removed, the required receiver gain must be distributed only on the mm-wave low-noise amplifier (LNA) and the baseband variable gain amplifier (VGA). However, with the same dc current consumption, the available gain for metal-oxide-semiconductor field-effect transistor (MOSFET) operating at mm-wave frequencies is relatively low. The maximum available gain rolls off as frequency increases. On the other hand, linearity issue limits the maximum gain allocated on the baseband VGA. As a result, the key feature of low power consumption may not be valid.

Thirdly, mm-wave quadrature frequency source and mixing component are usually realized by quadrature voltage controlled oscillator (QVCO) and IQ mixer. Both of them increase the complexity of the receiver front end and the risk of failure that is due to inaccuracy modeling.

On the contrary, heterodyne receiver is regarded as a better solution for mm-wave receiver. For the receiver front end, heterodyne receiver reduces the complexity of the circuits that have to be operated at mm-wave frequencies. The remaining mm-wave frequency circuits in a heterodyne mm-wave receiver include a LNA, a mixer, and a VCO. However, for IQ demodulation, comparing to the direct-conversion receiver, which has to operate four phases at mm-wave frequencies, only differential signaling is required for the mixer and the VCO in a heterodyne receiver, and thus simplifies the circuit design. The IQ signals are obtained from second down-conversion, which is operated at a much lower intermediate frequency and the IQ mismatch problem is not as severe as the mismatch problem at mm-wave frequencies. Moreover, reasonable gain can be allocated at the IF amplifier, thus a better overall tradeoff between noise, linearity, and power consumption can be made for receiver optimization.

The dominant issue in a heterodyne receiver, as mentioned in Section 2.2.2, is the image frequency. The tradeoff between image rejection and channel selectivity affects the selection of LO frequency. Thanks to the frequency separation planning illustrated in Figure 2.2, channel selectivity specification is relaxed because each sub carrier is 2.16 GHz apart. Therefore, an IF around 10 GHz provides sufficient channel selectivity with the natural frequency response of the IF VGA, whereas the image frequency falls out of the 60-GHz band. Although there is less interferer in the millimeter wave spectrum, since

some proprietary or licensed communication systems use the band in the vicinity of the image frequency, the frequency response of the LNA should provide sufficient image rejection to omit the use of additional filters.

2.2.5 **Link budget calculation and specifications of the 60-GHz receiver front end**

In order to determine the specifications of the key components in the 60-GHz receiver front end, this section provides a simple link budget based on the assumption of short-range LOS link for low-power applications. The link budget in logarithmic form is given by [28]:

$$SNR = P_t + G_t - PL + G_r - P_N - IL\,, \tag{2.2}$$

where P_t is the transmit power, G_t and G_r are the antenna gains for transmitter and receiver, PL is the path loss, P_N is the noise power, and IL is the implementation loss. Fading is not considered here. In this calculation, it is assumed that binary phase-shift keying (BPSK) or quadrature phase-shift keying (QPSK) is used, therefore the theoretical signal-to-noise ratio (SNR) for a 10^{-6} bit error rate (BER) is 10.5 dB as illustrated in Figure 2.8. This sets a lower bound for the minimum sensitivity.

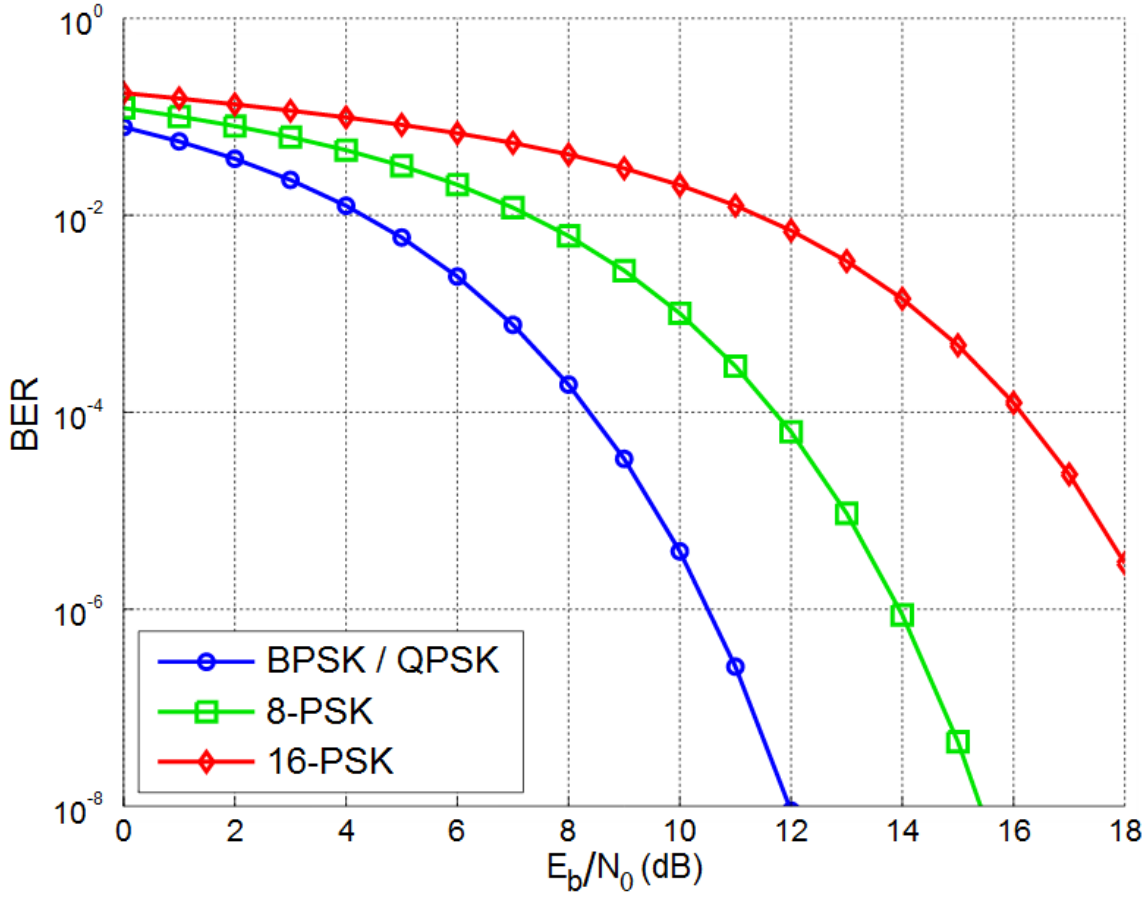


Figure 2.8. BER versus SNR curves plotted for BPSK, QPSK, 8-PSK and 16-PSK in AWGN channel [Online] Available: http://en.wikipedia.org/wiki/File:PSK_BER_curves.svg.

The transmit power P_t is usually low because of the limited performance of mmW CMOS power amplifier. Although CMOS mmW PA with output power of 20 dBm has been demonstrated, low efficiency (<15%) makes it dissipate more than 0.6 W and not suitable for low-power applications [46]. A practical value for P_t of 4 dBm is assumed here based on the information given in [47].

Antenna gain is assumed to be 8 dBi for both transmit and receive antennas. Although some of the state-of-the-art CMOS mmW receivers use high gain horn antennas, they

have difficulty for planar module integration [11], [13]. On the other hand, Bond-wire antenna featuring compact integration exhibits low gain, therefore they are only applied in in-module interconnect applications [34], [44]. As a tradeoff, patch antenna providing around 8-dBi gain appears to be most proper choice for low-power 60-GHz receiver front end.

Path loss *PL* in equation (2.2) can be derived from equation (2.1), taking a logarithmic form of the third term in equation (2.1), we get

$$PL = 20\log\left(\frac{\lambda}{4\pi R}\right). \tag{2.3}$$

Given that the wavelength at 60 GHz is 5mm, the path loss of a 1 meter LOS link is 68 dB.

The noise power term P_N presented in equation (2.2) is given by

$$P_N = 10\log(kBT) + NF = 10\log(kT) + 10\log(B) + NF, \tag{2.4}$$

where k is the Boltzmann constant, $1.38\text{x}10^{-23}$, in Joule/K, T is the absolute temperature in Kelvin, B is the bandwidth occupied by the RF signal, and NF is the noise figure of the receiver. At room temperature, equation (2.4) can be simplified as

$$P_N = 10\log(kBT) + NF = -174dBm + 10\log(B) + NF, \tag{2.5}$$

Given the channel bandwidth for 60-GHz standards is 2.16 GHz from Figure 2.2 and a practical receiver noise figure of 10 dB, the noise power is -71 dBm.

The last term of equation (2.2) is the implementation loss. Implementation loss comes from the imperfection of the real receiver such as phase noise of the local oscillator and nonlinear distortion of the front end. An empirical value of 6 dB is assumed [48].

Adding all results derived above, the SNR can be obtained as 17 dB, which is larger than the minimum requirement of 10.5 dB, and therefore validates the assumptions of receiver front end specifications as summarized in Table 2.4. Moreover, since the obtained SNR is 6.5 dB larger than the minimum required SNR for BPSK and QPSK, the maximum coverage is around 2 meters.

The short range link is sufficient for 60-GHz wireless personal area network (WPAN). For a 60-GHz wireless local area network (WLAN) system, the coverage should be enhanced to 10 meters LOS. Therefore the path loss increases by 20 dB comparing to the 1 meter case. To accommodate the additional loss, the required system specification is also shown in Table 2.4.

Table 2.4. Parameters for link budget analysis.

Parameter	WPAN	WLAN	Unit
Modulation scheme and minimum required SNR	10.5 (for BPSK/QPSK)		dB
Transmit power (P_t)	4	10	dBm
Antenna gain (G_t and G_r)	8	15	dBi
LOS Path loss at 1 meter coverage	68	88	dB
Bandwidth (B)	2.16	2.16	GHz
Receiver noise figure (NF)	10	10	dB
Noise power (P_N)	-71	-71	dBm
Implementation loss (IL)	6	6	dB
Resulting SNR	17	17	dB
Maximum coverage	2	20	meters

CHAPTER 3: DEVICE MODELING AT MM-WAVE FREQUENCIES

3.1 Introduction

Mm-wave receiver front-end circuits, including LNAs, mixers, and VCOs, consist of active and passive devices. The active devices, which refer to the transistors, provide the functions of amplification or frequency translation. The passive devices, which refer to lumped elements such as inductors and capacitors and distributed elements such as transmission lines, provide the functions of filtering, resonating, or impedance matching. At mm-wave frequencies, the foundry-provided models for both active and passive devices may be not accurate enough for successful front-end circuit designs and usually cause performance degradation in the first-round tapeout. Therefore, it is necessary to develop dedicated mm-wave models for both the passive and the active devices. In the mean time, mm-wave front-end circuits must be designed for robustness with respect to modeling inaccuracies. As a first step for mm-wave receiver front end design, the modeling methodology for both passive and active components will be discussed in this chapter.

3.2 Passive Components Modeling

The passive components used in mm-wave front-end circuits can be divided into two categories: lumped elements and distributed elements. Take mm-wave tuned amplifiers as an example, lumped-element design approach, which features a small footprint and a reduced silicon area [59], uses inductors in the matching network. Generally, foundry-provided inductor models are not applicable because the inductors

used at mm-wave frequencies are usually around 100-pH, which are much smaller than the minimum value of the foundry-provided inductor models. Electromagnetic (EM) simulator [49] or equation-based inductor/transformer simulators [50] are required to characterize the customized small inductors. However, since the inductors are implemented by the topmost metal layer without shielded ground planes using the lowest metal layer to isolate the lossy silicon substrate, the characteristic of the inductors are difficult to be predicted by software because of the lack of well-defined substrate dielectric constant and thickness. Amplifiers designed with lumped-element design approach usually experience frequency shift resulting from the inaccuracy of the inductor model [59] and need to be corrected in the next tapeout. An alternative solution is to build an inductor database in the first tapeout and model those inductors based on the measurement for future designs [51]. However, none of the lumped-element design approaches can achieve a first-pass design. It not only increases the cost and time but also reduces the flexibility for porting between different foundries.

On the other hand, the distributed-element-matched amplifier, which uses transmission lines in the matching network, usually needs a relatively larger silicon area. However, transmission lines have well-defined signal and ground planes. The electric field is confined between the signal and the ground, and therefore the transmission line characteristic can be predicted well before silicon implementation. The details will be described in the following paragraphs.

3.2.1 **Transmission line structures used in mm-wave front end**

According to the multi-layer planar structure of the CMOS back end of line (BEOL) interconnect metallization, two transmission line structures are commonly used:

thin-film microstrip line (TFMS) and grounded coplanar waveguide (GCPW) as shown in Figure 3.1. Both TFMS and GCPW feature perfect isolations to the lossy substrate. The electric field is well-confined between the signal line and ground, and therefore the characteristic can be predicted accurately by EM simulation software. In the proposed design approach, TFMS is chosen as the matching element because of the compact area. The TFMS along with the dc blocking and ac decoupling capacitors are the only three passive elements that need to be modeled in the proposed design methodology. A systematic modeling methodology is developed in this research for accurately predicting the high frequency characteristics with minimum hardware implementation.

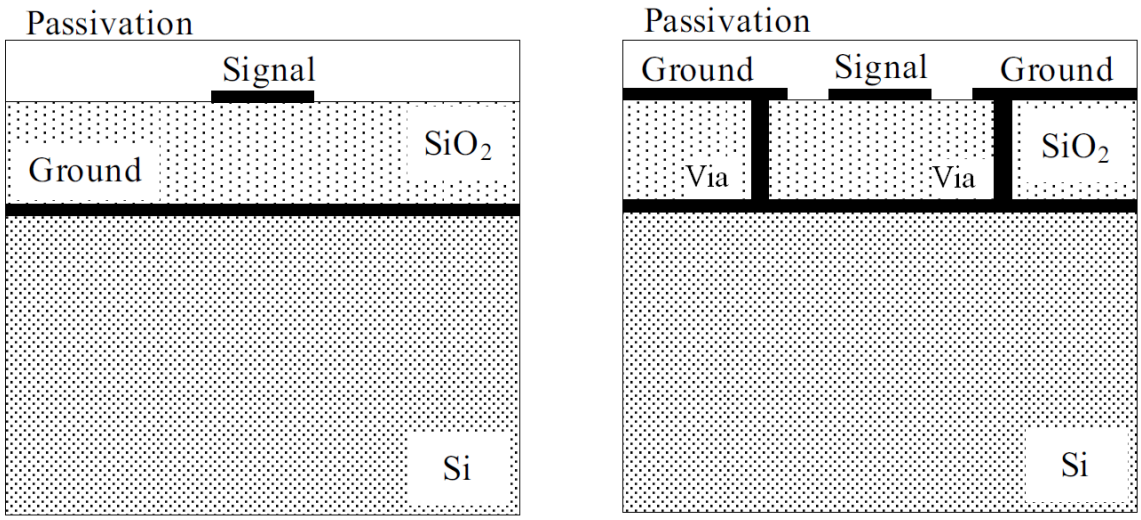


Figure 3.1. The structures of (a) Left: TFMS and (b) Right: GCPW on bulk CMOS processes.

It is worth mention of the ground plane in the TFMS. In most CMOS technologies, design rules limit the metal density of each metal layers. For instance, the maximum metal density for TSMC 65-nm 1P7M CMOS technology is 80% in a 20 μm x 20 μm window [54]. To satisfy the design rule, a complete and continuous ground plane with no

holes is prohibited. A common solution is to design a small square pattern with a square hole in the middle, which satisfies the density rules locally, then duplicate this pattern to form the whole ground plane. However, this method creates holes on the ground plane and thus increases the loss of transmission line. Figure 3.2 shows the EM simulation results of a 12-μm 50-Ω TFMS with and without patterned-hole ground plane. As summarized in Table 3.1, at 60-GHz, the amplitude error is 0.2% and phase error is 2.8%. For most circuit simulation that can tolerate this error, such as matching networks for amplifier, ideal ground plane can be used to replace the patterned-ground plane to drastically reduce memory and time for EM simulation. However, for certain critical circuit that highly relies on accurate amplitude and phase (e.g. phase shifters), simplification of the ground plane in EM simulators may result in deviations that degrade circuit performances. Moreover, some special transmission line design techniques utilize unique ground plane patterns to reduce the phase velocity, which is so-called “slow-wave” transmission line. Therefore, when the millimeter-wave signal propagates through the slow-wave transmission line, the effective guided wavelength is shortened. The required phase shift can be obtained with a smaller physical length. The sizes and losses of passive structures can be reduced by using slow-wave transmission lines [55]. Nevertheless, because of the physical size reduction, slow-wave transmission lines are more vulnerable to process variation. The special structures also increase the required accuracy of EM simulation and therefore become more sensitive to modeling inaccuracies. It is due to the research goal of this dissertation that a simpler TFMS structure is chosen instead.

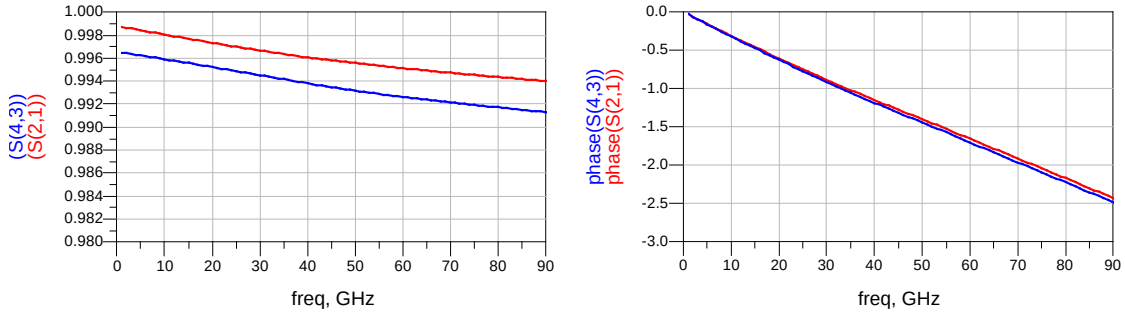


Figure 3.2. EM simulation results of amplitude (left plot) and phase (right plot) of a 12-μm TFMS with patterned-hole ground plane (blue curves) and ideal complete and continuous ground plane (red curves).

Table 3.1. EM simulation summary at 60 GHz of a 12-μm TFMS with patterned-hole ground plane and ideal complete and continuous ground plane.

Parameter	Ideal	Patterned-holes	Unit
Amplitude	0.995	0.993	N/A
Amplitude in dB	0.042	0.064	dB
Amplitude error	0.2		%
Phase	1.660	1.708	Degree
Phase error	-2.8		%

3.2.2 **Thin-film microstrip line (TFMS) modeling**

Scalable transmission line model is essential for circuit design. Unfortunately, unlike GaAs processes, foundry-provided transmission line models are usually not available in CMOS processes. Even though some foundries provide transmission line models, most of them are developed for low frequency applications and do not have flexibility on the transmission line structure (e.g. IBM's coplanar waveguide (CPW) transmission line model for digital interconnection assessment). Thus, before designing circuits, a scalable model for TFMS transmission line needs to be established. The general concept is finding a global model with behaviors conforming to individual

samples. The following procedure shows how to establish a scalable TFMS transmission line model.

First, the characteristic impedance Z_0 of the TFMS should be determined. 50 ohm is usually used as system interface impedance.

To establish a TFMS model for a given Z_0 (50 ohm in this case), the physical structure, which means the signal metal width and the distance between top metal signal line and bottom ground plane, must be determined. Closed-form equations can provide an approximate initial guess [53]. Commercial software such as Linecalc eases the calculation. Take the 1P7M 65-nm CMOS process for instance, the signal line is implemented at the top metal (M7) and the second layer (M2) is used as ground plane while M1 is reserved for power-supply and digital-control routings. In this scenario, the distance between signal line and ground is determined by the process as 3.4 μm. Therefore, the corresponding signal line width is 5 μm for 50 ohm impedance.

The structure of TFMS should be simulated and verified via EM simulation. An accurate EM simulation environment is essential. Fortunately, the well-defined ground plane isolates the substrate effect, thus simplifies the dielectric stack setup in EM simulators because the dielectric layers below the ground plane can be neglected. The stacked dielectric layer setup is based purely on the foundry-provided interconnection information [54]. Since the foundry-provided interconnection information usually have detailed dielectric constant and thickness for all the dielectric layers between metal layers but rarely have the information for the substrate because of the digital circuit design requirements, this simplification not only reduces the required simulation time but also

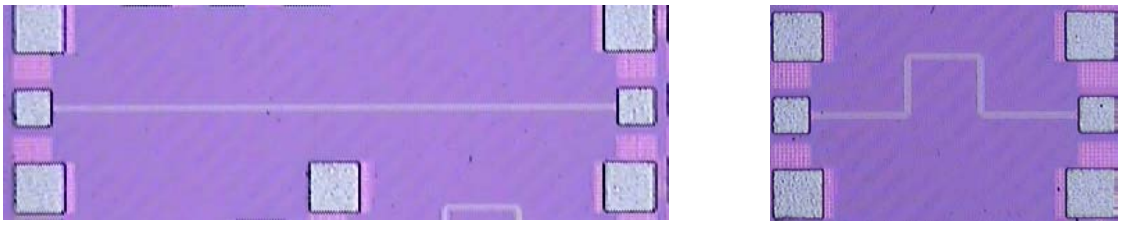
increases the accuracy by skipping the need of substrate information. In this case, TFMS with different lengths are first simulated by Sonnet to provide enough data points for the next modeling step [49].

By the S-parameters collected from simulating TFMS structures with different lengths, we can use the closed-form-equation-based transmission line models to fit the EM simulation results. In this case, the EM simulation results are modeled by using Agilent Technologies' Advanced Design System (ADS) microstrip multilayer substrate model [56]. The essential parameters for the multilayer substrate model are the characteristic impedance Z_0 and the relative dielectric constant ε_r. It also starts with the foundry-provided interconnection information and then fit the closed-form-equation-based model to the EM results with tweak.

90 degree bends and T junctions in TFMS are also simulated and modeled using equivalent models in ADS. The unified 90 degree bend and T junction structures are used in the circuit design. In fact, T junction causes negligible discontinuous effects while 90 degree bend is effectively less phase shifting than its physical length. Therefore, T junctions can be neglected while 90 degree bends can be modeled as shorter transmission lines in the schematic level.

This procedure demonstrates a simple method to model transmission lines for a given structure. Behaviors of different lengths are easily predicted by the model, thus ease the overall circuit design without multiple iterations between the circuit simulator and the EM simulation software. To validate the modeling procedure, the model is compared with the measurement of the test structure. Figure 3.3 shows the die photo of

two TFMS test structures that are both 5 μm in width but 990 μm and 560 μm in length, respectively.



(a) (b)

Figure 3.3. Die microphotograph of the transmission line test structures: (a) the straight 990 μm line, and (b) the 560 μm bend line.

In the measurement, an off-chip standard calibration kit is used for line-reflect-reflect-match (LRRM) calibration. As shown in Figure 3.4, pads and feeding structures are deembedded using ABCD matrices [53].

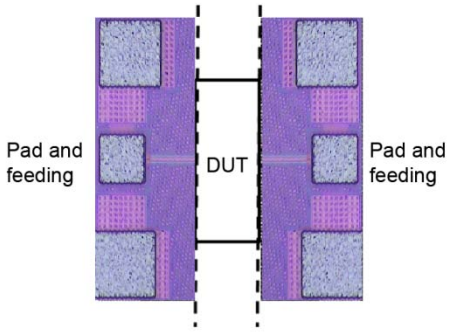


Figure 3.4. The test structure used in ABCD deembedding

Figure 3.5 shows model verification results of the TFMS, which reasonable agreement between model and measured results are achieved with a phase error < 3^{o} and amplitude error less than 0.1 dB at 60 GHz.

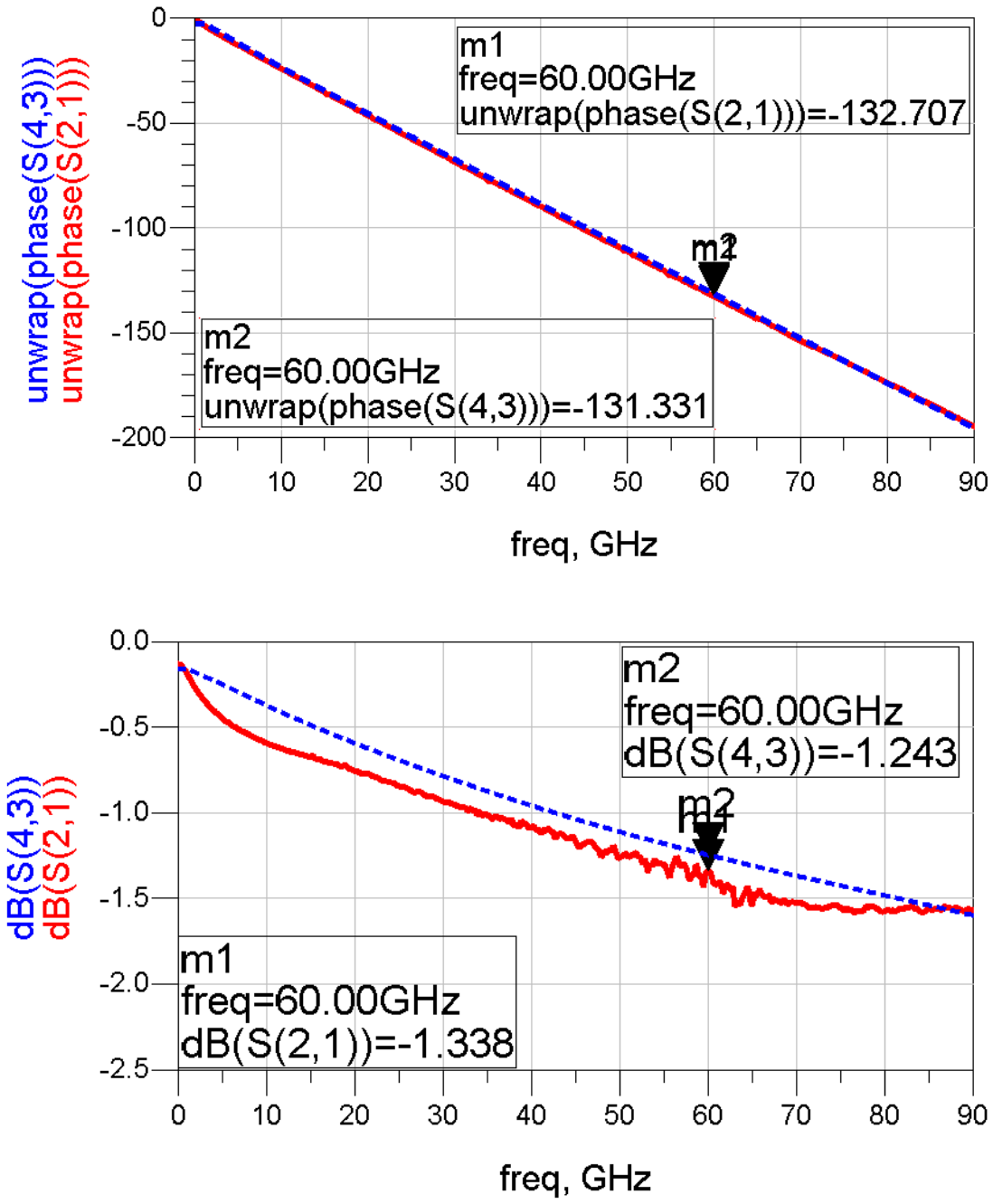
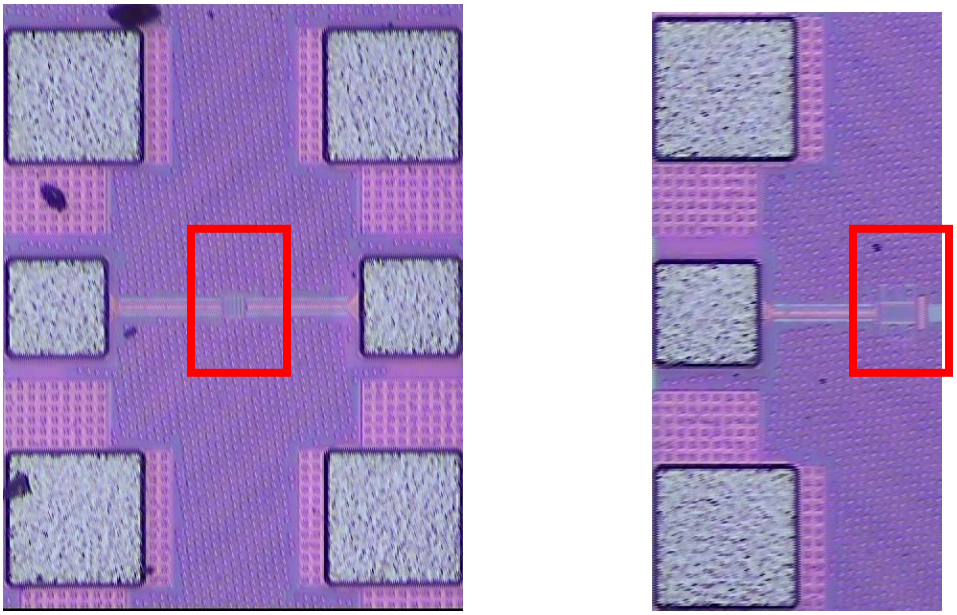


Figure 3.5. The 990 μm transmission line modeling. (S(4,3) in dot curves: EM simulation. S(2,1) in solid curves: Measurement; Top: phase, and bottom: magnitude.)

3.2.3 **Metal-insulator-metal (MIM) capacitor modeling**

The metal-insulator-metal (MIM) capacitors used as dc blocking and ac decoupling capacitors are also very critical for mm-wave amplifier designs. The foundry-provided model is based on the low frequency two port S-parameter measurements of several MIM capacitors that are different in geometries. The measurements are fit to high order regression equations without physical meanings. Although the capacitance can be estimated pretty well up to mm-wave frequencies, the parasitic inductance is ill-predicted at the frequency of interest. Test structures photo of a 250 fF dc-blocking capacitor and an 800 fF ac-decoupling capacitor are shown in Figure 3.6.



(a) **(b)**

Figure 3.6. Die microphotograph of the capacitor test structures: (a) dc-blocking and (b) ac-decoupling capacitors.

One- and two-port S-parameters are measured and also deembedded using the aforementioned ABCD matrix method for the ac-decoupling and dc-blocking capacitors. The comparison of the models and the measurements are shown in Figure 3.7.

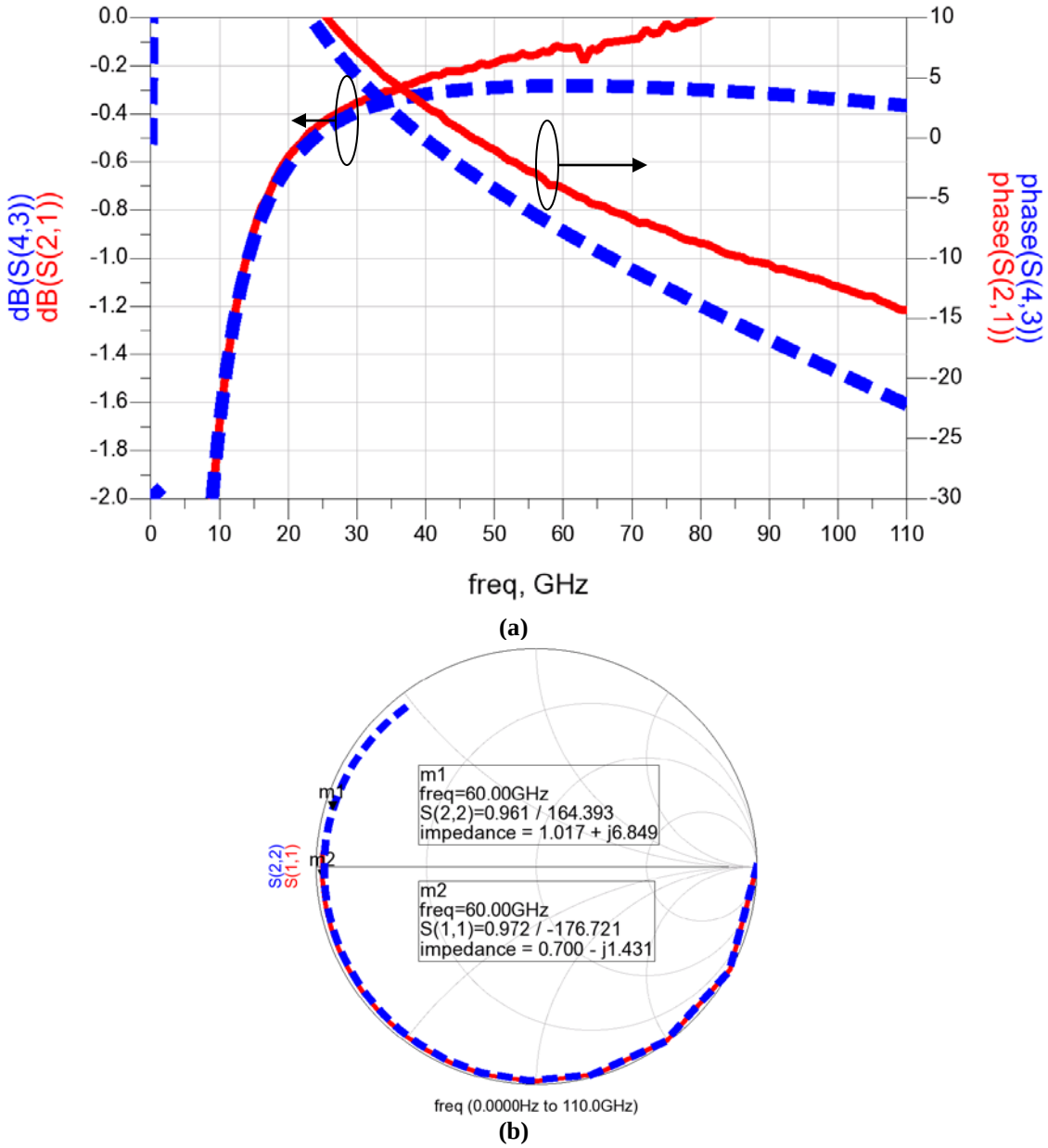


Figure 3.7. Comparison of the foundry-provided MIMCAP model to the measurement (Measurement: red solid curves. Model: blue dotted curves): (a) dc blocking capacitor (S(2,1) magnitude and phase) (b) Input impedance of the ac decoupling capacitor.

It can be found obviously that the models are accurate below 30 GHz, but errors are growing larger above 30 GHz and cannot be ignored at 60 GHz. The modified models are based on the foundry-provided MIM capacitor models with excess negative inductors

added at the input of the ac-decoupling capacitor for curve fitting at mm-wave frequencies. The sign is negative to cancel out the overestimated parasitic inductance of the foundry-provided model. Similar negative inductances are added at both terminals of the dc-blocking capacitor because it is used as a two-port element in the circuit design.

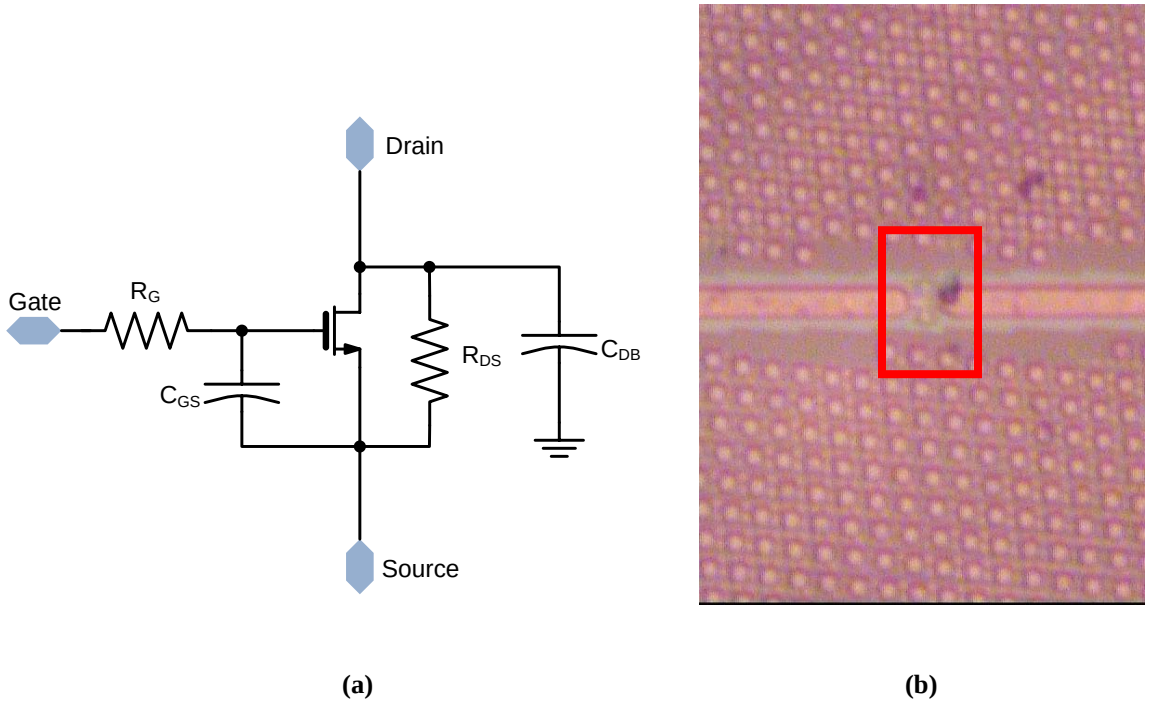
3.3 Active devices modeling

The accuracy of the transistor model is the most critical factor of mm-wave front-end circuit design. Since a pre-measured mm-wave S-parameter is not available, the foundry-provided transistor model is carefully analyzed to take the possible modeling inaccuracy and uncertainty into consideration. The first typical discrepancy source of the foundry-provided model is the gate resistance R_G. For analog or low frequency circuit design, the input impedance looking into the gate of the MOSFET is very large (similar to an open terminal), the small R_G is insignificant. Therefore, the small R_G is usually not well modeled by the foundry. However, at mm-wave frequencies, the gate capacitance of several tens of fento-Farads results in finite impedance and the series R_G becomes significant. The estimated gate resistance can be calculated with the equation given in [59]:

$$R_G = \frac{R_{GSQ} \cdot W_f}{3N_F \cdot l_g} + \frac{R_{CONT}}{N_{CONT} \cdot N_F} + \frac{R_{GSQ} \cdot l_{access}}{l_g}, \tag{3.1}$$

where R_{GSQ} is the gate sheet resistance per square, W_f is the finger width, N_f is the number of fingers, l_g is the finger length, R_{CONT} is the gate contact resistance, N_{CONT} is the number of gate contacts, and l_{access} is the gate contact to active distance. For a 40 μm total width device, the R_G is around 5 to 20 Ω regardless of the layout. The foundry-

provided 40-μm-width NMOS model shows a R_G of 15 -25 Ω depends on the number of fingers and the finger width. Other possible modeling inaccuracy, which includes the excess gate to source capacitance (C_{GS}), the excess drain to bulk capacitance (C_{DB}), and the parallel drain resistance (R_{DS}), are also considered in the NMOS transistor model for mm-wave design. The NMOS model is shown in Figure 3.8(a).



(a) **(b)**

Figure 3.8. (a) NMOS model used in the simulation. (b) NMOS test structure die microphotograph.

The model is compared with the measurement result of a 40-μm-width NMOS transistor with 40 fingers (W/L=40/0.06). The die microphotograph of the test structure is shown in Figure 3.8(b). The simulation results of both foundry-provided model and the enhanced mm-wave MOSFET model as well as the measurement results are plotted in Figure 3.9. With R_G= -6.5 ohm, C_{GS}=0, C_{DB}=5 fF, and R_{DS}=1 kΩ, the enhanced model can fit well to the measurement results and therefore validates the feasibility of the mm-wave enhanced model.

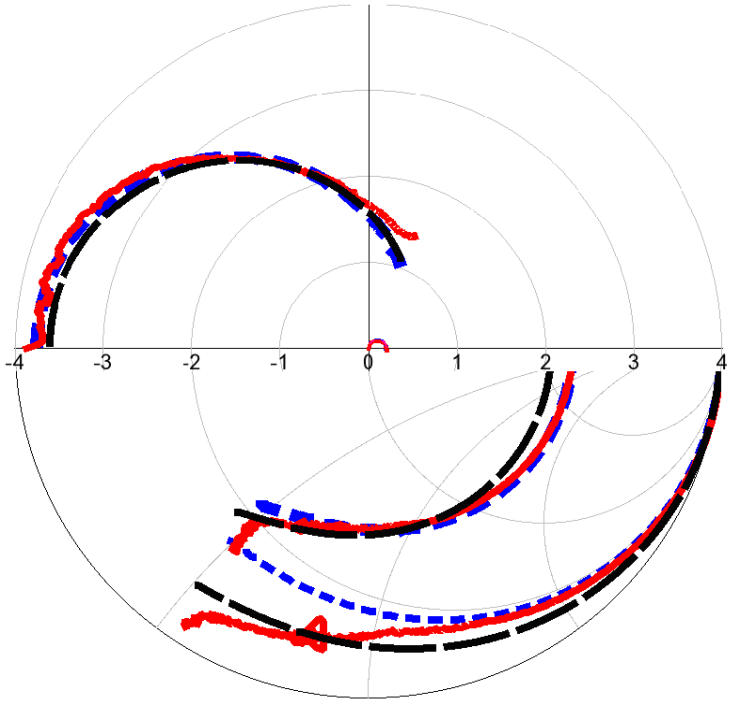


Figure 3.9. Comparison of the transistor model and the measurement (Measurement: red solid curves; Foundry-provided model: blue dot curves; Enhanced model: black long-dash curves): Lower-half plane: S(1,1) and S(2,2), and upper-half plane: S(2,1) and S(1,2). Frequency range is 1 – 110 GHz.

3.4 Summary

In this chapter, the modeling of both passive components and active devices used in CMOS millimeter-wave front-end design is introduced. Since transmission line models are usually not provided by the foundry, a step-by-step procedure for modeling TFMS in CMOS technology is elaborated firstly. Secondly, for foundry-provided models, including the capacitors and the transistors, the discrepancies of the model and measurement at millimeter-wave frequencies are analyzed. Additional lumped components are inserted to enhance the model accuracy to be applicable for mm-wave front end design. All modeling techniques are validated by measurements of 65-nm CMOS test structures.

CHAPTER 4: MM-WAVE LOW-NOISE AMPLIFIER DESIGN

4.1 Fundamentals of Low-Noise Amplifier

4.1.1 **Introduction**

Amplification is one of the basic and essential RF circuit function. The low noise amplifier (LNA) usually serves as the first stage of the receiver front end. The function of a LNA is amplifying the weak RF signal received by the antenna while minimally degrading the signal-to-noise ratio (SNR). The basic two key parameters for a LNA are gain and noise figure, which will be described in the following paragraph. Moreover, stability should be checked as first priority to ensure no oscillation signal will be generated by the LNA itself.

4.1.2 **Gain and stability**

Electrical circuits can be characterized by the relationship of voltage and current of the external ports. At low frequency, the z, y, h, and ABCD parameters are used widely. Nevertheless, at microwave or millimeter-wave frequencies, the short and open circuit tests are difficult to perform. The scattering parameters (S parameters) are introduced to characterize networks operating at microwave or millimeter-wave frequencies. In this section, several expressions for gain and stability of a general two-port amplifier will be introduced in terms of the S parameters of the transistor as a prerequisite for mm-wave LNA design [52]-[53].

4.1.2.1 Two-port power gains

Consider and arbitrary two-port network with s parameters [S] connected to source and load impedances Z_S and Z_L, respectively, as shown in Figure 4.1. In general,

the input impedance of the terminated two-port network will be mismatched with a reflection coefficient given by Γ_{in}, which can be determined using a signal flow graph shown in Figure 4.2. Similarly, the reflection coefficient seen at port 2 when port 1 is terminated by Z_S can also be derived, which labeled as Γ_{out}. Γ_{in} and Γ_{out} are derived as follows:

$$\Gamma_{in} = S_{11} + S_{21}S_{12}\Gamma_L + S_{21}S_{12}\Gamma_L^2 S_{22} + S_{21}S_{12}\Gamma_L^3 S_{22}^2 + \cdots = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1-\Gamma_L S_{22}} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}. \quad (4.1)$$

$$\Gamma_{out} = S_{22} + S_{21}S_{12}\Gamma_S + S_{21}S_{12}\Gamma_S^2 S_{11} + S_{21}S_{12}\Gamma_S^3 S_{11}^2 + \cdots = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1-\Gamma_S S_{11}} = \frac{Z_{out} - Z_0}{Z_{out} + Z_0}. \quad (4.2)$$

Before introducing several power gain equations, it is important to clarify the definition of "delivered power" and "available power". At the input port, the power delivered into the two-port network is denoted as P_{in}. To take account the source mismatch, the "power available from source" P_{avs} is defined as the power delivered into the two-port network when Z_{in} is conjugate matched to the source impedance Z_S and can be represented as:

$$P_{avs} = P_{in}\big|_{\Gamma_{in}=\Gamma_S^*}. \quad (4.3)$$

At the load termination, the power dissipated in the load is denoted as P_L. Similarly, the "power available from network" P_{avn} is defined as the power delivered to the load when the load impedance is conjugate matched to Z_{out}. That is,

$$P_{avn} = P_L\big|_{\Gamma_L=\Gamma_{out}^*}. \quad (4.4)$$

Three power gain equations are used most often: the operating power gain G_P, The available power gain G_A, and the transducer power gain G_T. The definitions and expressions are shown as follows:

$$G_P = \frac{P_L}{P_{in}} = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} = f(\Gamma_L) \quad . \tag{4.5}$$

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2 \frac{1}{1-|\Gamma_{out}|^2} = f(\Gamma_S) \quad . \tag{4.6}$$

$$G_T = \frac{P_L}{P_{avs}} = \frac{(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-S_{11}\Gamma_S - S_{22}\Gamma_L + \Delta\Gamma_S\Gamma_L|^2}|S_{21}|^2 = f(\Gamma_S, \Gamma_L)$$
$$\text{where } \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.7}$$

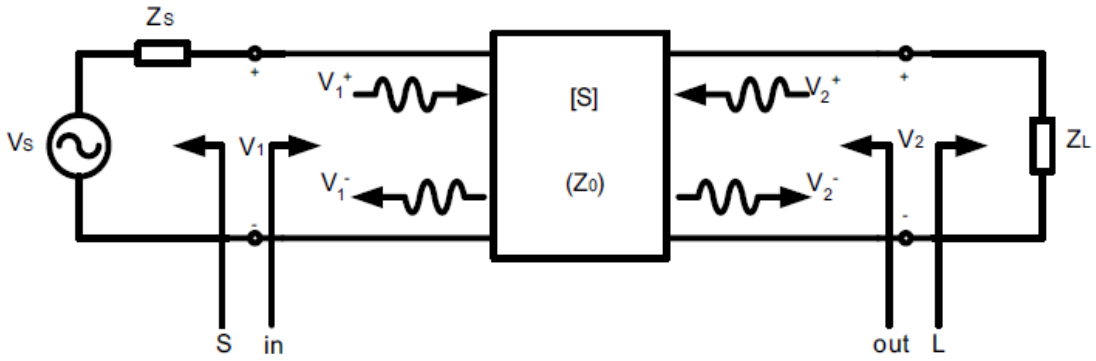


Figure 4.1. A two-port network with general source and load impedances.

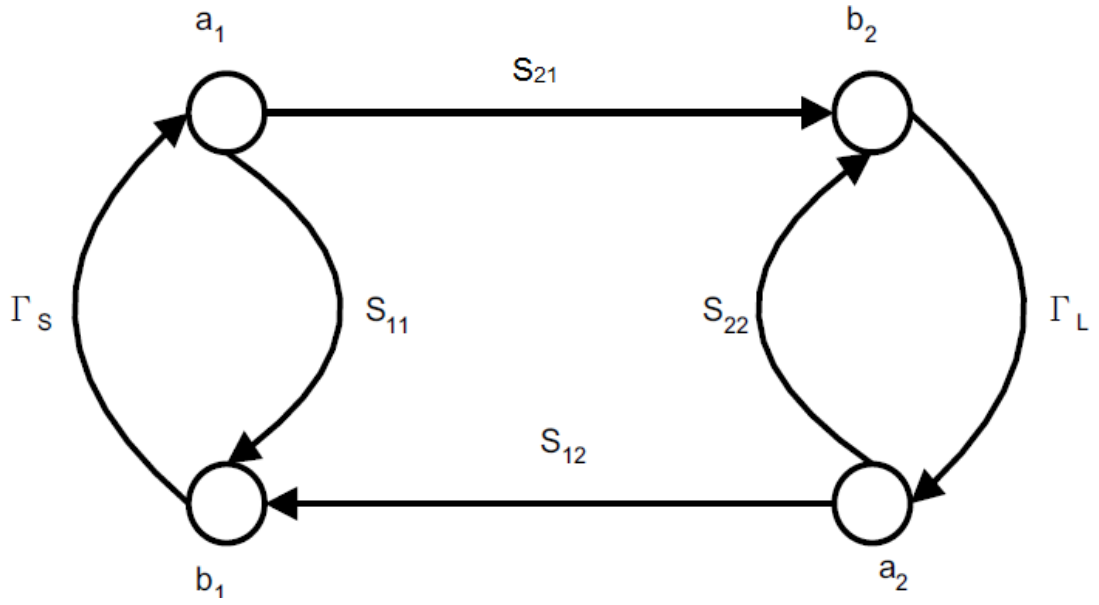


Figure 4.2. Signal flow graph representation of a two-port network.

4.1.2.2 Stability

An amplifier may oscillate if either the input or output impedance has a negative real part. According to (4.1) and (4.2), this implies that $|\Gamma_{in}|>1$ or $|\Gamma_{out}|>1$. From (4.1), Γ_{in} is a function of the S parameters and the reflection coefficient caused by the load impedance. From (4.2), Γ_{out} is also a function of the S parameters and the reflection coefficient caused by the source impedance. Therefore, if a set of S parameter can ensure that under all possibilities of source and load impedances, $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are kept smaller than unity, the amplifier with this set of S parameter is unconditionally at this frequency. This is the basic concept of Rollet's stability factor. The stability factor K is defined as:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|}$$
$$\text{where } \Delta = S_{11}S_{22} - S_{12}S_{21} \qquad (4.8)$$

For most solid-state transistor amplifiers, $|\Delta|$ is less than unity. Therefore, K>1 means the amplifier is unconditionally stable while K<1 means the amplifier is potentially unstable.

4.1.2.3 Transducer power gain

Consider a general single stage amplifier shown in , three different expressions of power gain equations (4.5)-(4.7) can be used. Among the three equations, only (4.7) depends on both Γ_S and Γ_L. At microwave frequencies, the input and output matching seriously affect the amplifier performance. Therefore, transducer power gain (4.7) is preferred for microwave transistor amplifier design.

Rearrange (4.7), we get

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} = G_S G_0 G_L$$
$$\text{where } G_S = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}$$
$$G_0 = |S_{21}|^2$$
$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad (4.9)$$

If the input/output matching networks satisfy $\Gamma_S=\Gamma_{in}^*=\Gamma_{MS}$ and $\Gamma_L=\Gamma_{out}^*=\Gamma_{ML}$, the transducer power gain reaches its maximum of

$$G_{T,\max} = \frac{1}{1-|\Gamma_{MS}|^2}|S_{21}|^2\frac{1-|\Gamma_{ML}|^2}{|1-S_{22}\Gamma_{ML}|^2} = \frac{|S_{21}|}{|S_{12}|}(K-\sqrt{K^2-1}), \qquad (4.10)$$

where K is the Rollet's stability factor given by (4.8). (4.10) estimates the gain performance of a transistor. For CMOS transistors, stability factors are less than unity at

low frequencies, indicating they are potentially unstable. The maximum gain for the amplifier without oscillation is defined as maximum stable gain (MSG) and can be obtained by setting K=1 in

$$MSG = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \quad . \tag{4.11}$$

Empirically, MSG rolls off with a slope of 3 dB/octave (10 dB/decade). After a transition frequency for K=1, the transistor becomes unconditionally stable. The maximum gain can be obtained at unconditionally stable condition is defined as maximum available gain (MAG) and can be derived as follows:

$$MAG = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \quad . \tag{4.12}$$

Empirically, MAG rolls off with a slope of a slope of 6 dB/octave (20 dB/decade). An example of typical MSG and MAG versus frequency is plotted in. It is worth mention that the frequency when MAG equals to unity (0 dB). The frequency is defined as maximum oscillation frequency (f_{max}). This is a figure of merit to determine the maximum operating frequency for amplifiers and oscillators. Moreover, higher f_{max} usually indicates higher MSG or MAG at the operating frequency. Nevertheless, it is also proven that even with some feedback techniques to obtain higher gain for a given transistor at a certain frequency, f_{max} remains unchanged [57].

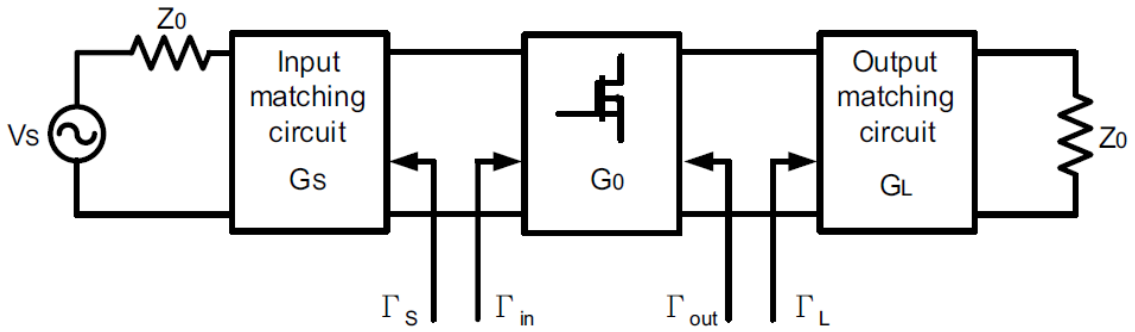


Figure 4.3. A general single-stage amplifier circuit schematic.

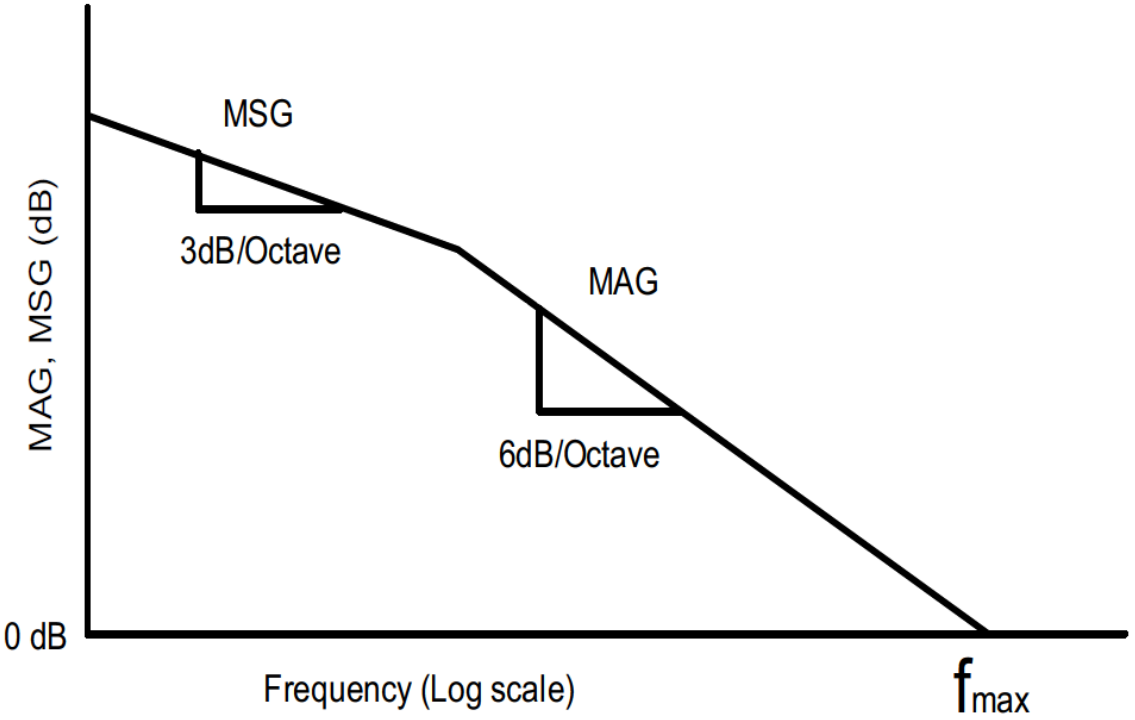


Figure 4.4. Typical MSG and MAG versus frequency plot.

4.1.3 **Noise**

Low noise amplifier is the first block of the receiver front end, which amplifies the weak incoming RF signal received by the antenna. However, the LNA itself contributes noise as well and therefore it should be designed with a compromise between maximizing its gain and minimizing its noise. The essential noise background is introduced in the section.

4.1.3.1 Noise types

Thermal Noise is the basic type of noise. It is discovered by Schottky in 1918 and first measured by Johnson in 1928. Thermal noise is generated by random thermal motion of electrons in resistive elements. These random motions produce small random voltage fluctuations. The square mean of this voltage is

$$\overline{v_t^2} = \frac{4hfR\Delta f}{e^{hf/kT} - 1}, \tag{4.13}$$

where h=6.546x10^{-34} J-sec is the Planck constant, k=1.380x10^{-23} JK^{-1} is Boltzmann constant, R is the resistance in Ω, and T is the absolute temperature in K. f and Δf denote the center frequency and the bandwidth, both are in Hz.

In most cases, $f << kT/h$. Therefore,

$$\begin{aligned} & e^{hf/kT} - 1 \cong \frac{hf}{kT}, \\ & \text{thus } \overline{v_t^2} = 4kTR\Delta f, \\ & \text{and } \overline{i_t^2} = \frac{4kT\Delta f}{R}, \end{aligned} \tag{4.14}$$

which can be modeled as series voltage source or shunt current source.

Shot Noise is generated by the random emission of electrons or by the random passage of electrons and holes across a potential barrier. The shot noise generated in a device can be modeled as a shunt noise current source. The square mean of shot noise current is

$$\overline{i_{sh}^2} = 2qI\Delta f, \tag{4.15}$$

where q=1.6x10^{-19} coulomb is electron charge, I is dc current in amperes, and Δf is the noise bandwidth in Hz.

Flicker Noise occurs in all solid-state components. In semiconductor, it is mainly caused by traps associated with contaminations and crystal defects. These traps capture and release carriers randomly and lead to a noise signal with energy concentrating at low frequency. Flicker noise is modeled by a noise current source in parallel with a device. The square mean of flicker noise current is

$$\overline{i_f^2} = \frac{K_f I^m \Delta f}{f^n}, \tag{4.16}$$

where K_f is the flicker noise coefficient, I is dc current in amperes, Δf is the noise bandwidth in Hz at frequency f, m=0.5 to 2 is the flicker noise exponent, and n is a constant about unity. Flicker noise is inverse proportional to frequency such that it is also called 1/f noise. It reveals that flicker noise dominates the low frequency noise while thermal noise contributes most noise above the corner frequency. The flicker noise corner frequency (f_c) is defined as the frequency that the noise is twice of the thermal limit. For submicron CMOS transistors, f_c is in the megahertz range. Thus, flicker noise can be neglected in millimeter-wave LNAs. However, it is crucial for oscillator phase noise because of the noise conversion mechanism.

4.1.3.2 Noise in CMOS transistors

In MOSFET, the channel induced is resistive, and therefore the principal noise type is thermal noise. The channel thermal noise is given by

$$\overline{i_{nd}^2} = 4kT\gamma g_{ds0}\Delta f \quad , \tag{4.17}$$

where g_{ds0} is the conductance at V_{DS}=0 V and γ is the channel thermal noise coefficient. γ=2/3 for long channel devices with gate lengths larger than 1 μm; For submicron devices, it is found that γ is larger than unity and is bias-dependent [58].

Furthermore, two additional noise sources are included in the MOSFET noise model. The gate thermal noise is generated by parasitic gate resistance R_G and can be derived as

$$\overline{v_{ng}^2} = 4kTR_G\Delta f \quad . \tag{4.18}$$

Another noise source is caused by the shot noise formed by gate leakage current I_G, which can be derived as

$$\overline{i_{ng}^2} = 2qI_G\Delta f \quad . \tag{4.19}$$

As a consequence, the model for MOSFET including the aforementioned three types of noise is illustrated in Figure 4.5.

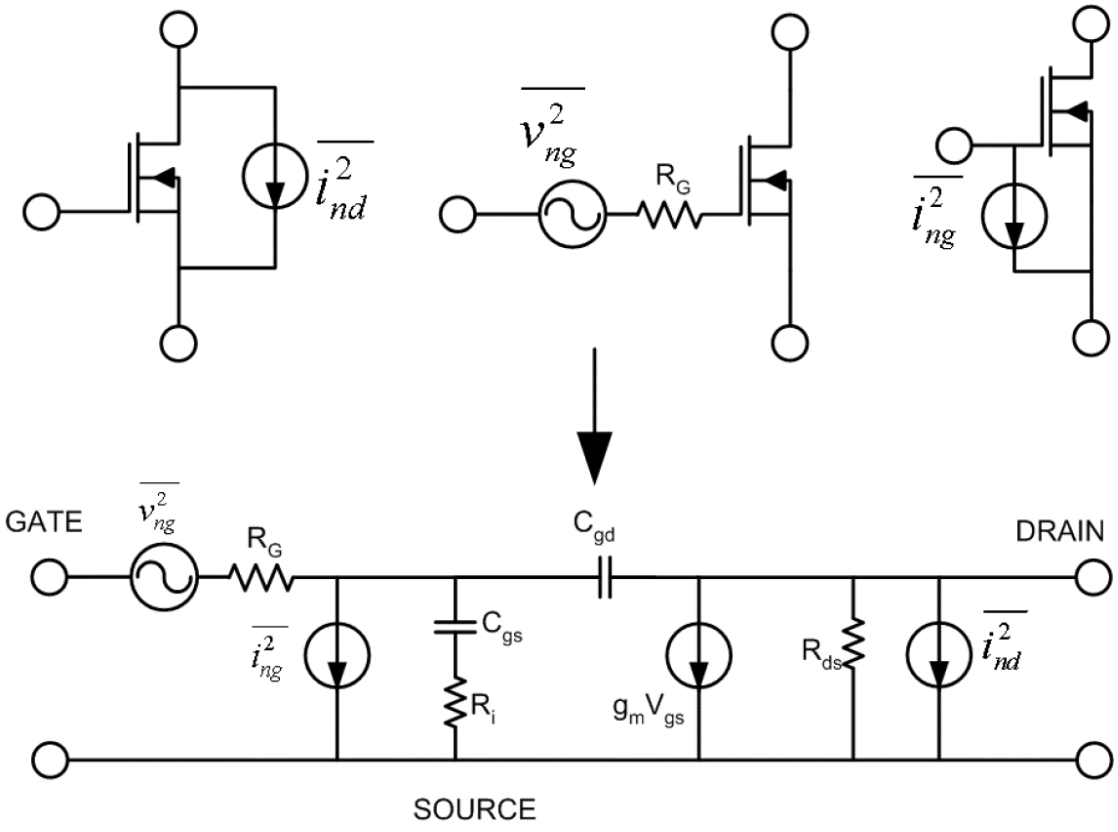


Figure 4.5. Noise model for CMOS MOSFET.

4.1.3.3 Noise factor and noise figure

To quantify how the signal-to-noise ratio (SNR) degrades for a two-port network, noise factor is defined as the ratio of input SNR to output SNR. As illustrated in, noise factor can be derived as

$$F = \frac{\text{input SNR}}{\text{output SNR}}$$

$$= \frac{S_i / N_i}{S_o / N_o}$$

$$= \frac{S_i / N_i}{GS_i / G(N_i + N_{DUT}|_{input-referred})}$$

$$= 1 + \frac{N_{DUT}|_{input-referred}}{N_i}$$

$$= 1 + \frac{\overline{(v_n + i_n R_S)^2}}{\overline{v_{nS}^2}} \quad . \tag{4.20}$$

Noise figure is noise factor represented in decibel. It is the common form we may find in literatures. The merit of noise factor is that it can be easily calculated when multiple stages are cascaded. Assume a two-stage amplifier with noise factor and gain of the first and the second stages are F_1, F_2 and G_1, G_2, respectively. Friis formula gives the overall noise factor F as

$$F = F_1 + \frac{F_2 - 1}{G_1} \quad . \tag{4.21}$$

The noise contributed by the second stage is diluted with the gain of the first stage. As a consequence, the first stage of LNA dominates the overall noise figure. A more general equation is shown below for multistage (N-stage) LNA design.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{\prod_{i=1}^{N-1} G_i} \quad . \tag{4.22}$$

4.2 Model Inaccuracy Aware Design Methodology

LNAs are operated at the highest frequency for an mm-wave transceiver. Therefore, a systematic design methodology of LNA is the key for a first-pass mm-wave transceiver design. In this section, the discrepancies between the foundry-provided models and the measured components are carefully analyzed and modeled as variables to be taken into consideration for the amplifier design. A 57-64 GHz LNA is designed as an example of the proposed methodology.

4.2.1 Parametric analysis of the discrepancy between the foundry-provided model and the measurement

Mm-wave models for both passive and active components used in the circuit design have been developed in Chapter 2. Additional parameters are added to the foundry-provided model to minimize the discrepancy between the foundry-provided model and the measurement result. The modified models contain variables represent the possible inaccuracy of the foundry-provided models at the frequency of interest. These variables are tabulated in Table 4.1. These variables are going to be used in a LNA design. The goal is to develop a design methodology for mm-wave LNA that ensures stability and reasonable gain and noise performances while highly accurate high frequency model is not available and discrepancies between the model and the reality always exists.

Table 4.1. List of variables for modeling inaccuracy.

Notation	Description	Range	Unit
R_G	Gate resistance error of the NMOS model	0 ~ -10	Ω
C_{GS}	Gate to source capacitance error of the NMOS model	0 ~ 10	fF
C_{DB}	Drain to bulk capacitance error of the NMOS model	0 ~ 10	fF
R_{DS}	Drain resistance error of the NMOS model	0.5 ~ 2	kΩ
K_{TLine}	Multiplying factor of the transmission line length	0.97 ~1.03	Unitless
$K_{\sigma sub}$	Multiplying factor of the substrate conductivity	0.8 ~ 1	Unitless
$L_{dc\_block\_cap}$	Series inductance error of the dc-blocking MIMCAP	0 ~ -2	pH
$L_{decouple\_cap}$	Series inductance error of the decoupling MIMCAP	0 ~ -6	pH

4.2.2 **Model-uncertainty-insensitive design approach**

The objective is to design an amplifier that can still meet the specifications under different combinations of modeling inaccuracies. A 60 GHz LNA is used as an example to elaborate the design methodology. The targeted bandwidth is 57-64 GHz with 20 dB gain. Four-stage common-source topology is chosen to satisfy the gain specification. Although cascode configuration has higher intrinsic gain, it is not favored in the proposed design methodology because the foundry-provided model is based on common-source transistor measurement, which provides a higher accuracy in the modeling. Furthermore, the real part of the output impedance of the cascode configuration is higher than the

common-source configuration. The high-Q characteristic usually results in a narrow-band matching and is more vulnerable to modeling inaccuracies.

Among all the variables listed in Table 4.1, R_G and $L_{decouple\_cap}$ affect the LNA input/output matching and the frequency response most. R_G can be viewed as a series resistor at the gate of the NMOS. Therefore, R_G has a strong effect on the stability. $L_{decouple\_cap}$ introduces an equivalent excess length of the shunt short stub, so the matching is affected. To cope with the problem, the LNA topology shown in Figure 4.6 is proposed.

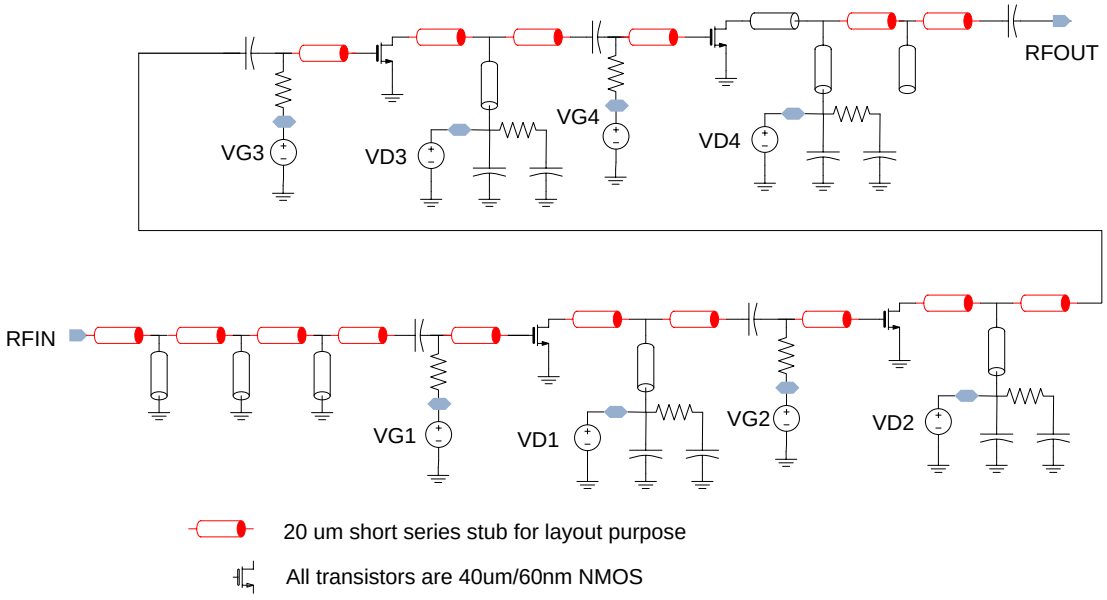


Figure 4.6. Schematic diagram of the modeling-inaccuracy-insensitive LNA.

Although the circuit schematic looks similar to conventional distributed-element-matched amplifiers with T-shape (two series transmission line and one shunt short stub) matching networks, two basic differences make the LNA very robust to the inaccuracies

of the models: (1) Series transmission lines are minimized, and (2) Removing the shunt short stubs at the gate terminals of all interstages.

(1) Series transmission lines are minimized:

For a lossless transmission line terminated by an arbitrary load Z_L, the input impedance looking into the transmission line is given as [53]:

$$Z_{in} = Z_0 \frac{Z_L \cos \beta l + jZ_0 \sin \beta l}{Z_0 \cos \beta l + jZ_L \sin \beta l}, \tag{4.23}$$

where Z_0 is the characteristic impedance, β is the phase constant, and *l* is the length of the transmission line. The impedance variation according to the variation of Z_L can be derived by taking a partial derivative of Z_{in} to Z_L.

$$\frac{\partial Z_{in}}{\partial Z_L} = \frac{Z_0^2}{(Z_0 \cos \beta l - jZ_L \sin \beta l)^2}. \tag{4.24}$$

Assume a simplified general case of 100 fF input capacitance with a corresponding Z_L of -27j at 60 GHz. A 45^o phase shift transmission line with 50 ohm Z_0 results in $\partial Z_{in} / \partial Z_L = 9.5$. The derivation shows that if a series transmission line is connected to the gate of the transistor, the inaccuracy of the transistor model is amplified at the input terminal. In order to achieve impedance matching without using series transmission line, device size needs to be properly chosen thus the input capacitance can be matched to 50 ohm by a single shunt inductor emulated by a shunt short stub. Fortunately, the selections of device width with proper gate capacitance are usually around 30 μm to 60 μm in 65 nm and 90 nm technologies. The device width of 30 μm to 60 μm is coincidentally to be

the optimum transistor size for LNA designs considering intrinsic gain and minimum noise figure. In the example design, NMOS size of W/L=40/0.06 with 40 fingers is selected for all four stages of the LNA. Unified transistor size simplifies the design of matching networks and biasing circuits.

(2) Removing the shunt short stubs at the gate terminals of all interstages:

Since the parasitic inductance of the decoupling capacitor introduces an undetermined excess length of the shunt stub, which is difficult to be modeled in the design phase, a straightforward solution is to minimize the use of the decoupling capacitors. Decoupling capacitors are used in shunt short stubs. Therefore, minimizing the use of shunt short stubs directly reduces the need of decoupling capacitors. For drain terminals of the transistors, short stubs are required for biasing. However, at the gate terminals, since there are no biasing dc currents flowing through the gate, the gate terminals can be biased with a large resistor. As shown in Figure 4.6, all interstages are simply loaded with a shunt short stub at the drain, acting as an inductor, to tune out the total capacitances seen from the drain and the gate terminals. The stages are tuned with shunt stubs of slightly different lengths. The stagger tuning technique results in a wider bandwidth.

For the biasing of the transistor, by operating the transistor in a current density (J) zone where $\partial f_{\max}/\partial J$ and $\partial NF_{\min}/\partial J$ are minimized, the effect of variation on process corners can be alleviated. An empirical optimum J=0.15 mA/μm is given by [59]. Therefore, the transistor is biased with constant current of 6 mA per stage. Total current consumption is 24 mA under a one-Volt supply voltage.

It is worth mentioning that the three parallel shunt short stubs used at the first-stage input-matching network. The aforementioned first guideline indicates that the input matching can be achieved with a simple short stub. However, short stub with ac-decoupling capacitor is not favored according to the second guideline. An alternative is to place the short stub before the dc-blocking capacitor. Therefore, the gate terminals can still be biased through a large resistor and the short stub can direct connect to ground. Therefore, the length of the short stub can be well predicted. Furthermore, the short stubs used at the LNA input terminal can be also used as electrostatic-discharge (ESD) path [60] - [61].

4.2.3 **Simulation results**

The LNA is simulated using GoldenGate^{TM}. Performances are predicted by post-layout simulation performed with the physical layout shown in Figure 4.7. A nested parametric sweep is used to simulate all possible combinations of the modeling inaccuracies tabulated in Table 4.1. The small signal gain (S(2,1)) and Noise figure are shown in Figure 4.8. Even though under different variable combinations of the modeling inaccuracies, a flat gain response better than 14 dB and a noise figure better than 7 dB can still be maintained. Figure 4.9 shows the input/output return losses that are better than 10 dB within 58 to 62 GHz for the worst case. Figure 4.10 shows that the Rollet's stability factors (K factor) are greater than unity for all situations. For definition of K factor, please refer to 4.1.2.2.

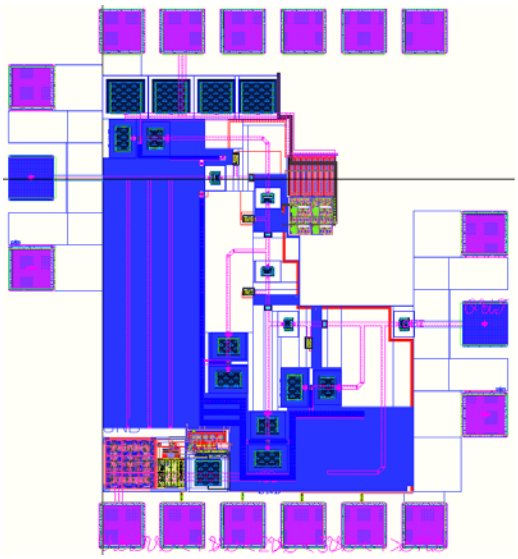


Figure 4.7. Physical layout of the modeling-uncertainty-insensitive 60-GHz LNA.

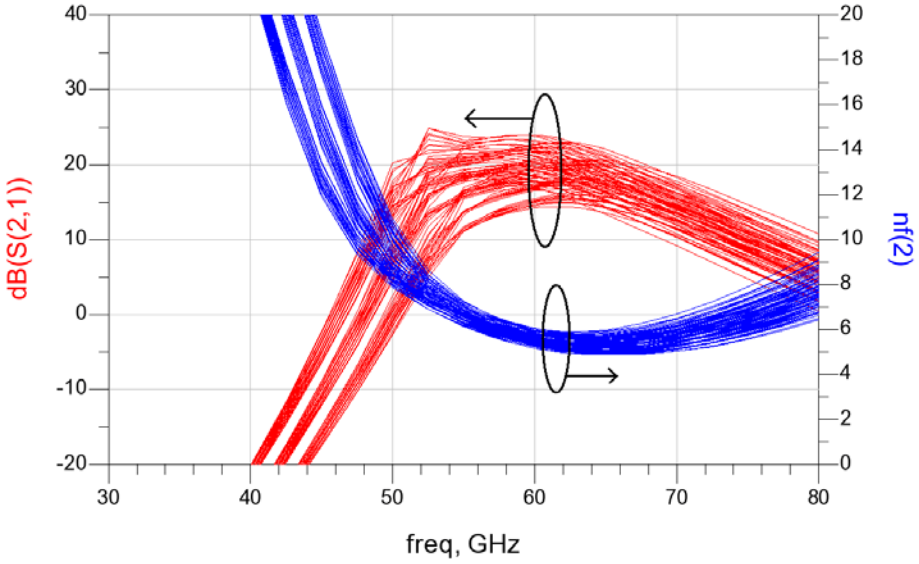


Figure 4.8. Simulated gain (S(2,1)) and noise figure of the LNA for 60 GHz operation in red and blue curves, respectively.

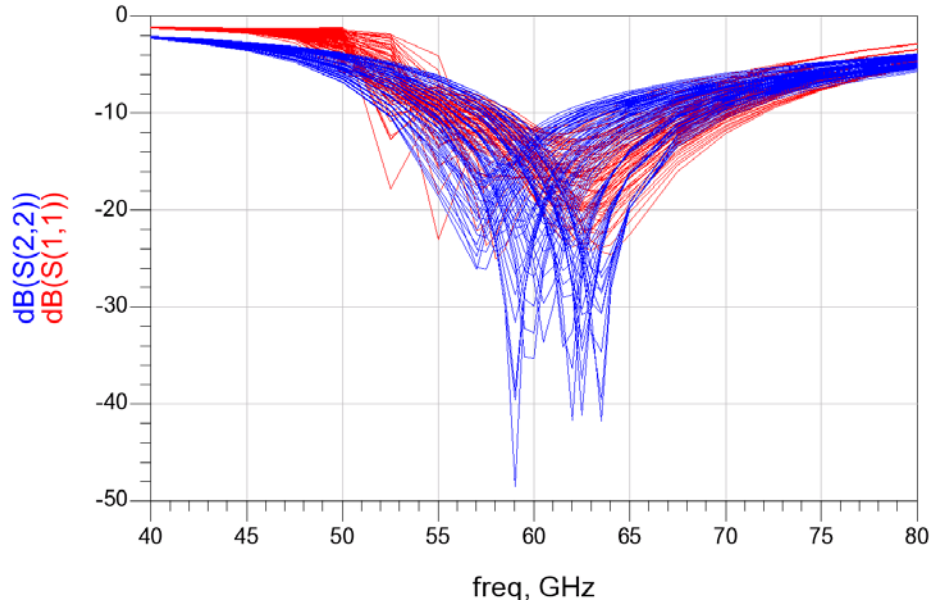


Figure 4.9. Simulated input/output return losses of the LNA (red curves: S(1,1), and blue curves: S(2,2)). Input return losses are always better than 10 dB from 58 to 62 GHz.

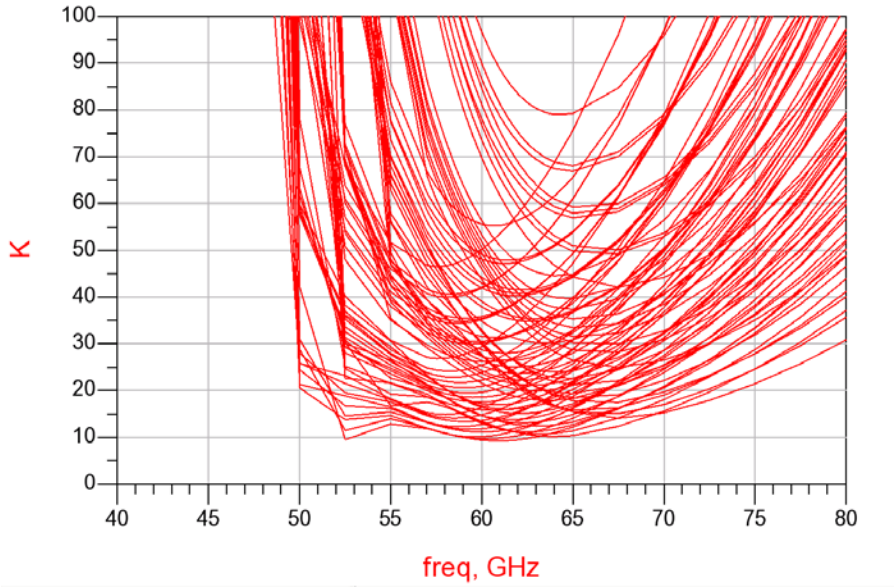


Figure 4.10. Simulated stability factor (K-factor) of the LNA.

Simulation results prove the robustness of the design methodology under reasonable variations of model parameters caused by inaccurate modeling at mm-wave frequencies. The input-referred third-order-intercept point (IIP3) and the input-referred 1-dB gain compression point (P_{1dB}) are -13 dBm and -21 dBm, respectively. The performance of the LNA proves that the proposed design methodology does not sacrifice the performance for the compromise of robustness.

4.3 Temperature Variation Compensation

By the aforementioned modeling-inaccuracy-aware design methodology, the LNA can be designed less sensitive to the modeling inaccuracies. However, temperature variation inherent to the CMOS technology still affects the performance of the LNA, and it becomes more stringent at mm-wave frequencies. This is due to the limited maximum available gain of CMOS transistors operating at mm-wave frequencies that the designers are forced to adopt multi-stage amplifier topology for obtaining sufficient gain. Therefore, the change of the transistor mobility caused by temperature variation results in significant degradation of the overall gain for the multi-stage cascaded LNA as well as its noise performance.

[59] and [62]-[66] report successful LNA designs operating around 60 GHz using CMOS technologies. Nevertheless, none of those mm-wave LNAs had been tested under a wide temperature range that satisfies typical industrial standards. Temperature variation performances were tested in [67]. The LNA shows 7 dB gain variation from -40 to 85 ^{o}C with 13 dB nominal gain at 27 ^{o}C. Temperature variation performances for mm-wave PAs were reported in [68]-[69]. But [68]-[69] didn't provide feasible solutions to minimize the performance variation. In summary, the temperature dependence

characteristic of the CMOS transistor strongly affects the performance of CMOS mm-wave amplifiers, but a practical solution to minimize the temperature effects is not yet developed.

4.3.1 **Temperature variation analysis for mm-wave LNA**

To simplify the temperature variation analysis, the scope is narrowed down to a single stage LNA. The analytic equation of the power gain G_P of a single-stage LNA [70] when biased at its peak f_T, in the approximation of $R_{ds} >> R_{load}$, can be approximated as

$$G_P \approx \frac{1}{4}\frac{g_m^{\,2}}{C_{gs}^2 \omega^2}, \tag{4.25}$$

where g_m and C_{gs} are the transconductance and gate-source capacitance of the transistor and ω is the operating frequency. According to this equation, G_P is a function of both g_m and C_{gs}. Since the change of C_{gs} is negligible when comparing to the change of g_m with respect to temperature variation [71], the relationship between G_P and the temperature can be derived from the transconductance-temperature dependence.

In CMOS devices, the temperature-dependent effects are mainly due to the threshold voltage and the mobility variation. According to [72], the threshold voltage of the CMOS device has a similar temperature tendency as the bipolar device with temperature coefficient (TC) of -2 mV/^{o}C. The carrier mobility decreases as temperature increases because of its exponential nature. The fractional temperature coefficient (TC_f) of the mobility is given as

$$TC_f = \frac{1}{\mu}\frac{\partial \mu(T)}{\partial T} = -1.5T^{-1} \quad . \tag{4.26}$$

The transconductance can be expressed as

$$g_m(T) = \mu(T) C_{ox} (\tfrac{W}{L})(V_{gs} - V_{th}(T)) \quad . \tag{4.27}$$

Since the mm-wave LNA is usually biased with constant gate-source voltage, the TC_f of g_m can be derived as

$$\begin{aligned} TC_f &= \frac{1}{g_m}\frac{\partial g_m(T)}{\partial T} = \frac{1}{\mu}\frac{\partial \mu(T)}{\partial T} - \frac{1}{V_{eff}}\frac{\partial V_{th}(T)}{\partial T} \\ &= -1.5T^{-1} + \frac{2\,mV/°C}{V_{eff}} \end{aligned} \quad , \tag{4.28}$$

where $V_{eff} = V_{gs} - V_{th}$ is the overdrive voltage of the common source stage. According to Equation (4.28), TC_f can be set to zero by proper selection of V_{eff}. This particular bias point is the zero-temperature-coefficient point of transconductance (ZTC_{gm}) [73]. However, the V_{gs} at ZTC_{gm} is usually very low. It is found that V_{gs}=0.46 V to satisfy the ZTC_{gm} criterion for a 130 nm process in [73], which is slightly higher than the threshold voltage. It can also be proved by (11) that a weak overdrive voltage at the denominator of the second term is required for $TC_f \approx 0$. A weak overdrive voltage is not the proper biasing point for mm-wave LNAs. The optimum biasing point is given by the optimum current density (J_{OPT}) for minimum noise figure of the NMOS. An empirical optimum value of $J_{OPT} \approx 0.15$ mA/μm is given in [59], which is independent of the CMOS technology or foundry. The transistor is biased in strong overdrive voltage to obtain J_{OPT}. According to Equation (4.28), when the transistor is biased in strong overdrive voltage, the first term dominates and thus g_m decreases as the temperature increases. This results in gain degradation as the temperature increases.

4.3.2 **Temperature-variation-compensated mm-wave LNA design**

The 60-GHz LNA was designed in a 90-nm 1-poly-7-metal (1P7M) bulk CMOS process. Four cascode stages are cascaded to obtain an overall gain higher than 20 dB. The matching circuit is realized with thin-film microstrip (TFMS) transmission lines. Figure 4.11 shows the schematic diagram of the LNA. TFMS is implemented using the top (M7) and the bottom (M1) metal layers as the signal line and the ground plane, respectively. Input and output ports are matched to 50 ohm while the interstages are conjugate matched to complex impedances. Stagger tuning technique is utilized to achieve a broad-band response.

The device size used in the LNA is selected to be 60μm/90nm, and thus the optimum bias current is 9 mA per stage. Although it is claimed by previous literature that the non-identical combination of the common-source (CS) and common-gate (CG) NMOS transistors leads to a higher Gmax and better gain and noise performances in cascode mm-wave LNA designs [62], identical device size of 60μm/90nm are selected for both CS and CG transistors in this design to obtain the same overdrive voltage and thus a uniform temperature coefficient according to Equation (4.28). As shown in Figure 4.11, the gate bias of the CG transistors are tied directly to VDD with a 2-kΩ resistor to ensure that V_{GS}=V_{DS} for both the CS and CG transistors. All biasing nodes at the short-stub ends are ac grounded by metal-oxide-metal (MOM) decoupling capacitors to provide protection against low-frequency oscillation.

A temperature-compensation bias circuitry is designed to bias V_{B1} to V_{B4} in Figure 4.11. The schematic diagram of the bias circuitry is shown in Figure 4.12. Bipolar transistors Q_1 and Q_2, an identical PMOS current source pair, and an operational

amplifier (opamp) form the proportional-to-absolute-temperature (PTAT) current generator. Since the current flowing through Q_1 and Q_2 are identical and the positive and the negative inputs of the opamp are virtually shorted, it can be derived that

$$I_{C1} = I_{C2} = \frac{V_T \ln(n)}{R_1}, \tag{4.29}$$

where n is the emitter area ratio of Q_2 and Q_1. Since V_T = kT/q, the collector current I_{C1} and I_{C2} are PTAT. The temperature coefficient can be controlled by the emitter area ratio n and the resistor R_1. The PTAT current is mirrored with M1-M4 to bias the LNA. The (W/L) of M1-M4 are 750 nm/90 nm to obtain 9 mA current for each stage of the LNA from 110 μA PTAT current generated by the bias circuitry. Figure 4.13 plots PTAT current temperature response with different process corners and ±10% power supply variation. The largest deviation comes from the process variation of the poly resistor (R_1) and thus results in three clusters of curves, which correspond to the three different process corners of the poly resistor (TT, FF, SS). To investigate the impact caused by the high variation poly resistor statistically, the result of the Monte Carlo simulation with 10K trials was plotted in Figure 4.14.

It can be found that although the resistor corners (FF and SS) show a significant deviation in Figure 4.13, the probability of falling into these corners is relatively low and thus the bias circuitry is applicable for the mm-wave LNA. Moreover, in order to test the performance variation of the mm-wave LNA with and without the biasing circuitry, biasing pads are added for V_{B1}-V_{B4}. By turning off the mirror branches M_1-M_4 with the bias selection pad (SEL_PAD) in Figure 4.12, VB1 to VB4 can be biased with external voltage supplies through biasing pads V_{B1}_PAD to V_{B4}_PAD.

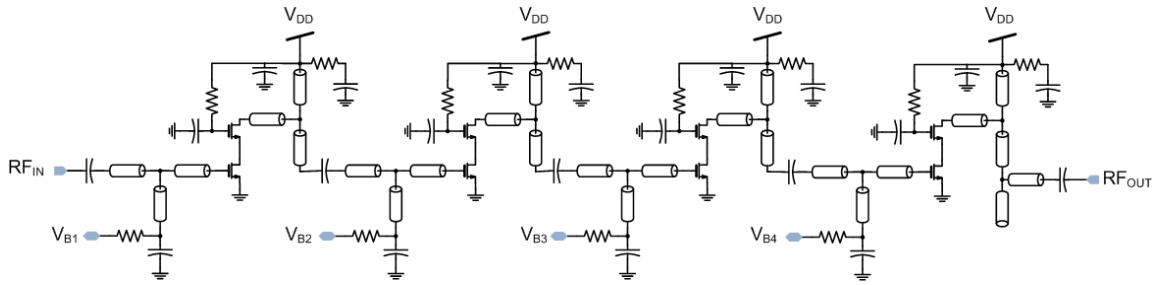


Figure 4.11. Schematic diagram of the temperature-compensated 60-GHz LNA.

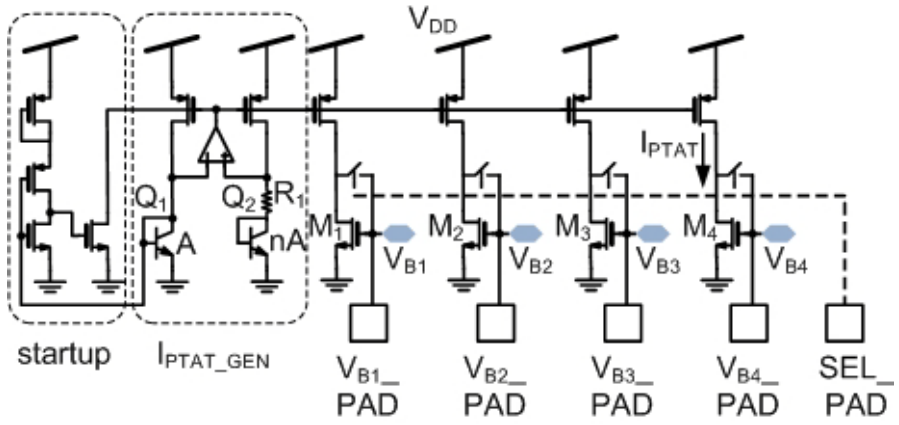


Figure 4.12. Schematic diagram of the temperature compensation bias circuitry.

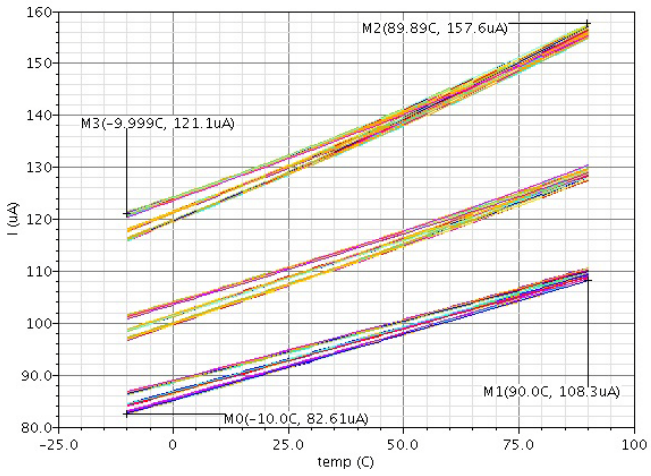


Figure 4.13. PTAT current temperature response with different process corners and ±10% power supply variation.

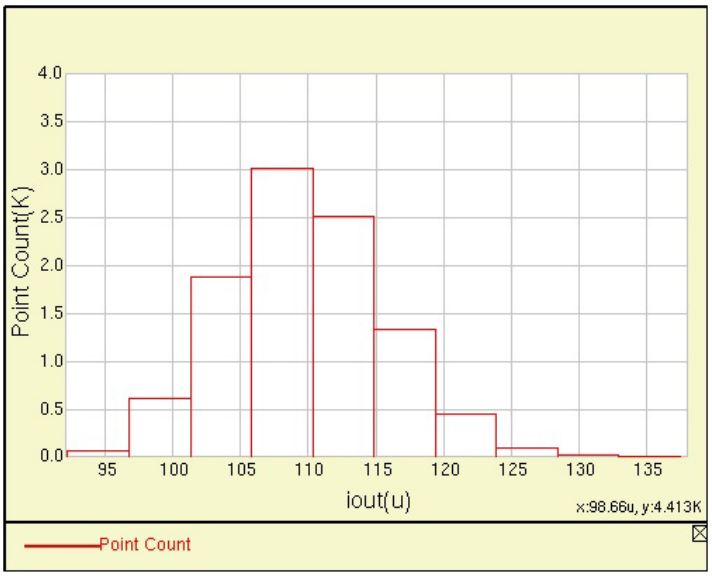


Figure 4.14. PTAT current variation with respect to process variation at 27 oC in 10K trials in histogram form.

4.3.3 **Experimental results**

Figure 4.15 shows the fabricated die microphotograph and the chip area is 1.06 mm^2 including test pads. The LNA is measured via on-wafer probing. The measured S-parameters and noise figure at 27^{o}C are shown in Figure 4.16. This measurement result is tested with the built-in bias circuitry, which provides bias voltage of 0.64 V for VB1 to VB4 under 1.3 V supply voltage and 49 mW dc power consumption. Identical S-parameter measurement results were also obtained by providing 0.64 V external bias voltages through biasing pads V_{B1}_PAD to V_{B4}_PAD. Thanks to the wide-band stagger-tuning technique, the measured gain is better than 18 dB from 55 to 64 GHz with a peak gain of 21 dB. The noise figure is around 6.5 to 8 dB within the same frequency band. The measured output-referred 1-dB compression point (P_{1dB}) and the input-referred third-order-intercept point (*IIP3*) at 60 GHz are -0.9 dBm and -11.1 dBm, respectively. The functionality of the temperature-compensation biasing is tested by measuring the LNA gain under temperature ranges from -5 ^{o}C to 85 ^{o}C, which is less than the temperature

range measured in [67] because of the equipment limitation. Figure 4.17 shows the |S21| at -5, 27, and 85 ^{o}C with and without the temperature-compensation biasing circuitry. It can be found that the proposed temperature-compensation biasing can significantly improve the gain variation under different temperature, especially for the gain degradation at higher temperature. The gain variation is confined within 5 dB with the temperature compensation biasing, whereas a variation of 10 dB is observed for constant voltage biasing.

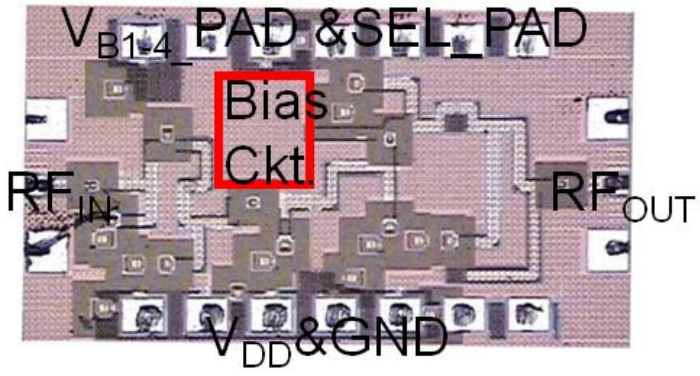


Figure 4.15. Die microphotograph of the temperature-compensated 60-GHz LNA.

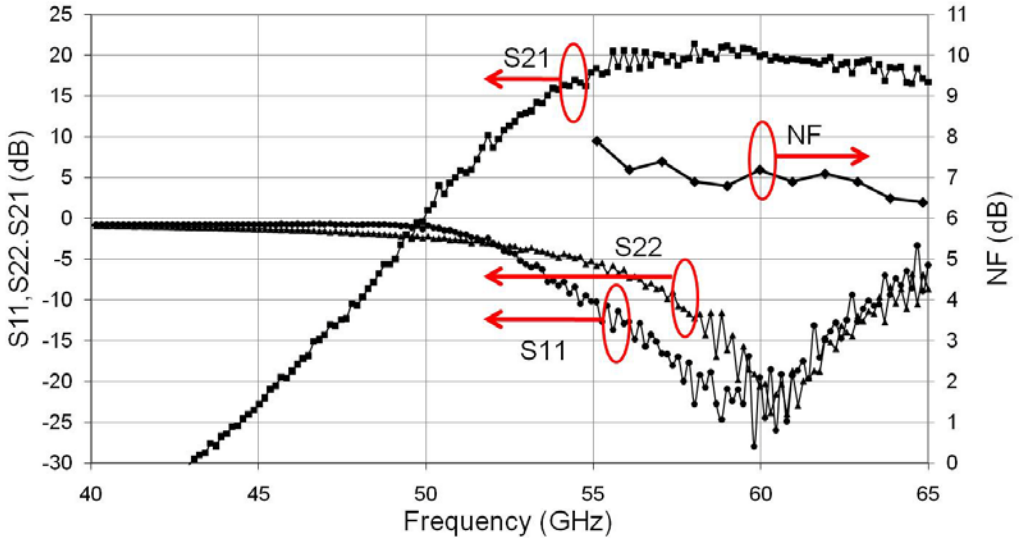


Figure 4.16. The measured S-parameters and noise figure of the LNA at 27^{o}C.

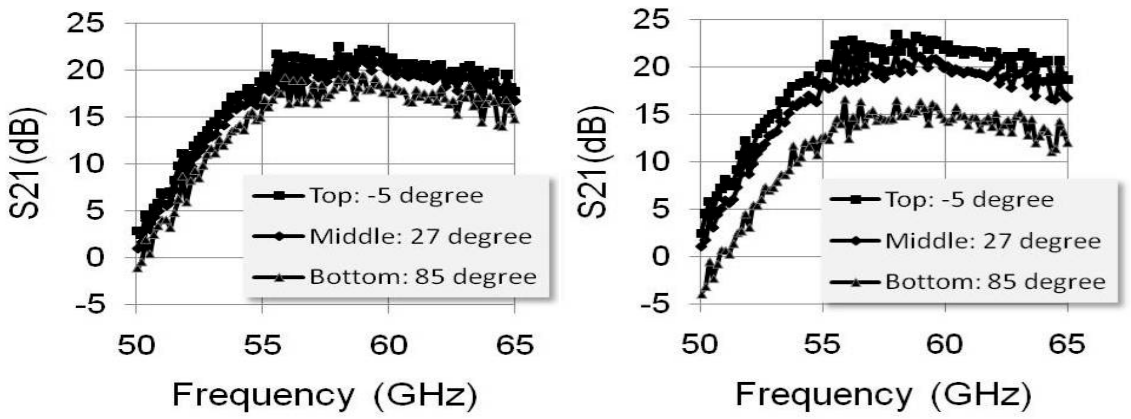


Figure 4.17. Measured LNA gain at -5°C, 27°C, and 85°C. (a) Left: with the temperature compensation biasing circuitry, and (b) Right: constant external voltage biasing.

4.4 Summary

This chapter summarizes the CMOS low-noise amplifier design used in an mm-wave receiver front end. The most essential knowledge of LNA design, such as gain and noise, are reviewed with mixture of conventional RF and microwave design approaches to build a solid fundamental. Based on the fundamental, two LNA design methodologies are introduced as treatments of modeling uncertainty and temperature variation.

Firstly, a modeling-uncertainty-insensitive LNA design approach is introduced. Starting with an analysis of the foundry provided model, possible inaccuracies are captured and modeled. Suitable LNA topology is proposed for tolerating the model uncertainties at mm-wave frequencies and validated by simulation with TSMC 65-nm CMOS design kit. It is proved that by this methodology, the required accuracy level for a successful mm-wave LNA design can be relaxed.

Secondly, a temperature-variation compensation technique for mm-wave MOS LNAs is proposed. The proposed technique is validated by measurement results of a 60-GHz LNA fabricated in a standard 90-nm CMOS process. The measured gain is more stable

over temperature variation with the proposed temperature-compensation biasing schemes. In terms of gain, noise figure, and power consumption, the temperature-compensated 60-GHz LNA presents comparable performances to the published state-of-the-art V-band LNAs [59], [62]-[67], which proves robustness and performance can be obtained simultaneously.

In conclusion, two 60-GHz LNAs are designed for mm-wave receiver front end in this chapter. Not only enables an operable low-noise amplification block in the front end, these methodologies also improve the robustness of mm-wave LNA designs against model inaccuracy and temperature variation without tradeoff in RF performance or power consumption. The performances of the mm-wave LNAs are tabulated in Table 4.2.

Table 4.2. Performance summary of the 60-GHz LNAs.

Specification	Modeling-uncertainty-insensitive 60-GHz LNA*	Temperature-variation-compensated 60-GHz LNA	Unit
Technology	65	90	nm
Topology	4-stage CS**	4-stage CC***	N/A
Frequency	60	60	GHz
Gain	20	21	dB
3-dB Bandwidth	54 – 68	55 - 64	GHz
Fractional Bandwidth	23	15	%
Noise Figure	5	6.5	dB
IIP3	-13	-11.1	dBm
Power Consumption	26	49	mW

* Post-layout simulation without silicon verification
**CS: Common-source
***CC: Cascode

CHAPTER 5: FREQUENCY GENERATION CIRCUIT DESIGN

5.1 Introduction

Frequency generation is a critical part in a receiver front end. In some conventional definitions, a RF receiver front end does not include frequency generation circuits. The local oscillator (LO) signal is fed externally with phase-locked loop (PLL) to stabilize it. However, at millimeter-wave frequencies, the passive components are small enough to be placed on chip. An on-chip mm-wave VCO can be integrated into the receiver chip. On the other hand, the inter-chip connection, either achieved by bond wire [74]-[75] or flip chip [76]-[77], induces additional loss at mm-wave frequencies. Therefore, fully-integration of the frequency generation circuits within the receiver front end not only reduces the cost but also improves the performance.

For the heterodyne receiver we adopted because of the aforementioned advantages in Section 2.2.4, two voltage-controlled oscillators (VCOs) are required: One for the LO of RF signal and another for the LO of IF signal. The RF VCO, or mm-wave VCO hereby, serves as the LO signal for the mixer that down converts the incoming mm-wave signal received by the antenna to the intermediate frequency (IF). Then, another VCO is used as the LO signal for down conversion from IF to baseband. This IF VCO has to provide quadrature phases for IQ demodulation. Therefore, the topology of quadrature VCO (QVCO) is adopted. In this chapter, the designs for both the mm-wave VCO and the IF QVCO will be discussed. Firstly, the IF QVCO will be introduced with emphasis on the causes and solutions of the inherent bimodal oscillation. Secondly, we will discuss the output power enhancement of the mm-wave VCO and its corresponding reliability

issues. An integrated VCO-mixer codesign is also proposed for optimization in both RF performances and reliability.

5.2 IF QVCO Design

5.2.1 The bimodal-oscillation phenomenon inherent to current-coupled QVCOs

QVCOs are widely used in radio frequency transceivers requiring in-phase and quadrature-phase (IQ) modulation/demodulation [78]-[79]. The topology of a conventional NMOS current-coupled QVCO is shown in Figure 5.1.

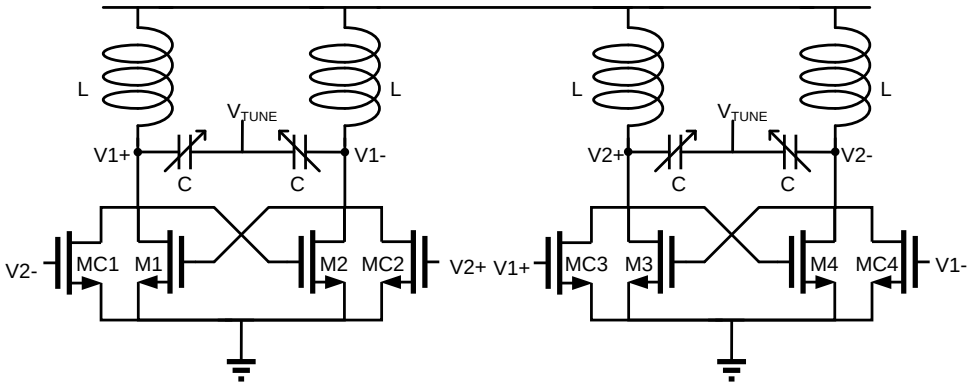


Figure 5.1. Schematic diagram of the conventional NMOS current-coupled QVCO.

This is the most widely used QVCO. Nevertheless, the conventional NMOS current-coupled QVCO suffers from the inherent bimodal-oscillation phenomenon, which is described mathematically in [80] and [81]. The phase ambiguity caused by the bimodal oscillation is crucial for an IQ modulator/demodulator. It may cause a degradation of the output power and can lead to stability issues in the PLL-based frequency synthesizer.

It will be reviewed in section 5.2.2 that the QVCO has two possible modes of operation in clockwise and counterclockwise rotations. This phase ambiguity results in

two possible steady-state oscillation frequencies. Such behavior is called the bimodal-oscillation phenomenon. However, [80] and [81] state that in practical implementation only one of the modes can sustain stable oscillation because of the asymmetric characteristic of the LC-tank-impedance frequency response. Nevertheless, S. Li et al. proved that the bimodal oscillation does exist in practice by observing a 10-GHz NMOS current-coupled QVCO, and provided an improved topology to eliminate the bimodal oscillation [82]. In addition, a generalized proof of the bimodal oscillation is given in [83] with a predictable tendency relating to the loss mechanism of the LC tank. Thus, the bimodal oscillation is considered to be one of the most critical factors related to the LC-based QVCO design, and it is very sensitive to design variables. However, the approach of tuning design parameters to avoid the bimodal oscillation is not full proof, as small variations in the simulation model, process, voltage, temperature and device mismatch can bring back the bimodal oscillation. The stochastic nature of the bimodal oscillation makes it even harder to avoid. In particular, this issue can be very crucial for a first-pass-success implementation.

Currently, there has not been any investigation on how to control the QVCO to oscillate in one of those two specific operating modes based on a set of initial conditions. In this work, for the first time, such QVCO control mechanism has been shown and verified by the measurement of a 13-GHz QVCO. This approach ensures a first-pass-success implementation of the targeted frequency synthesizer. Circuit designers can get rid of the threat of the bimodal oscillation by controlling it with the proposed methodology.

The detailed cause of the bimodal oscillation is discussed in Section 5.2.2. Section 5.2.3 provides a systematic measurement procedure to control the operating mode of the QVCO. Experiment results of the QVCO with the proposed control method are presented in Section 5.2.4, followed by a brief summary in Section 5.2.5.

5.2.2 **Analysis of bimodal oscillation**

In Figure 5.1, the four oscillation nodes (V1+, V1-, V2+, and V2-) can be characterized using simultaneous equations. The steady-state nodal equations of V1+, V1-, V2+, and V2- can be written as follows:

$$\begin{aligned} V1^{+} &= -(G_M V1^{-} + G_{MC} V2^{-}) Z(j\omega) \\ V1^{-} &= -(G_M V1^{+} + G_{MC} V2^{+}) Z(j\omega) \\ V2^{+} &= -(G_M V2^{-} + G_{MC} V1^{+}) Z(j\omega) \\ V2^{-} &= -(G_M V2^{+} + G_{MC} V1^{-}) Z(j\omega), \end{aligned} \tag{5.1}$$

where $V1^{+}$, $V1^{-}$, $V2^{+}$, and $V2^{-}$ are voltage phasors at these four nodes. G_M and G_{MC} are large signal transconductances of the cross-coupled transistors (M1 to M4) and the current-coupling transistors (MC1 to MC4), respectively. $Z(j\omega)$ is the equivalent half-circuit LC-tank impedance. Since $V1^{-} = -V1^{+}$ and $V2^{-} = -V2^{+}$, (5.1) can be simplified as

$$\begin{aligned} V1^{+} &= G_M Z(j\omega)(V1^{+} + {}^{G_{MC}}\!/_{G_M} V2^{+}) \\ V2^{+} &= G_M Z(j\omega)(V2^{+} - {}^{G_{MC}}\!/_{G_M} V1^{+}). \end{aligned} \tag{5.2}$$

The solution of Equation (5.2) yields that $V2^{+} = \pm jV1^{+}$. It means $V2^{+}$ can be either leading or lagging $V1^{+}$ by 90^{o}. The phasor diagram of Equation (5.1) is plotted in Figure 5.2.

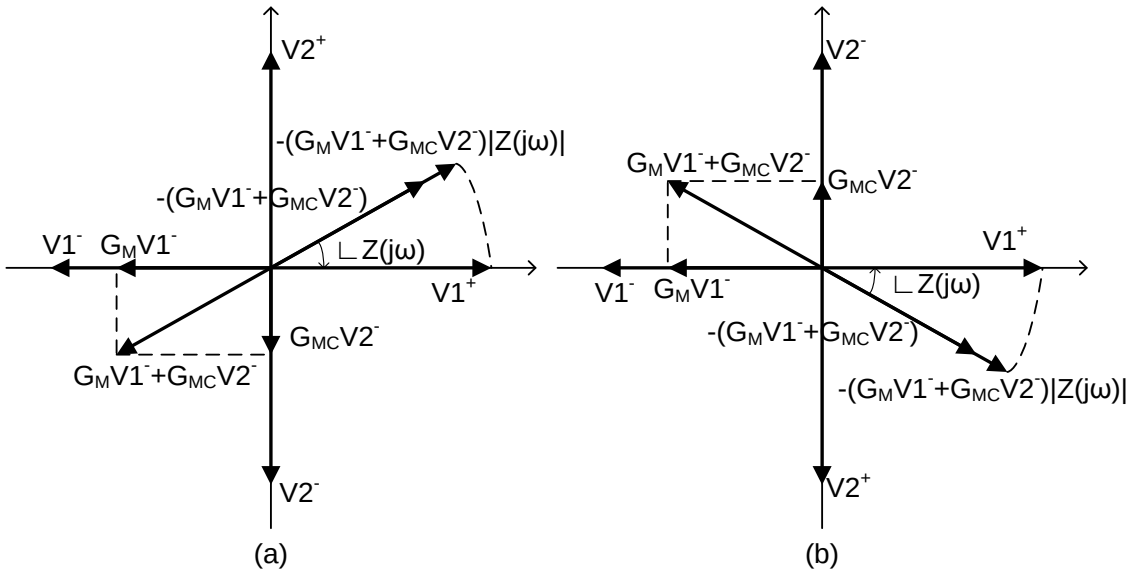


Figure 5.2. Phasor diagram of equation (6). (a) V2+ is leading V1+ by 90^{o}, and (b) V2+ is lagging V1+ by 90^{o}.

The injection currents of the coupling transistors (MC1 to MC4 in Figure 5.1) cause a phase shift from the original current vector and require a phase offset provided by the LC tank to compensate this phase deviation. As shown in Figure 5.2, the phase shift, $\angle Z(j\omega)$, provided by the LC tank, is equal to $\pm\tan^{-1}(G_{MC}/G_M)$. Using a 13-GHz QVCO design (with LC tank of 1 nH inductor and 150 fF capacitor) as an example, the widths of coupling transistors are chosen to be 1/4 of the cross-coupled-pair transistors. Thus, G_{MC} is roughly $G_M/4$, and that gives $\angle Z(j\omega) = \pm 14°$. Finite quality factors of the on-chip inductor and capacitor contribute to the asymmetric frequency response of impedance with respect to the resonance frequency shown in Figure 5.3.

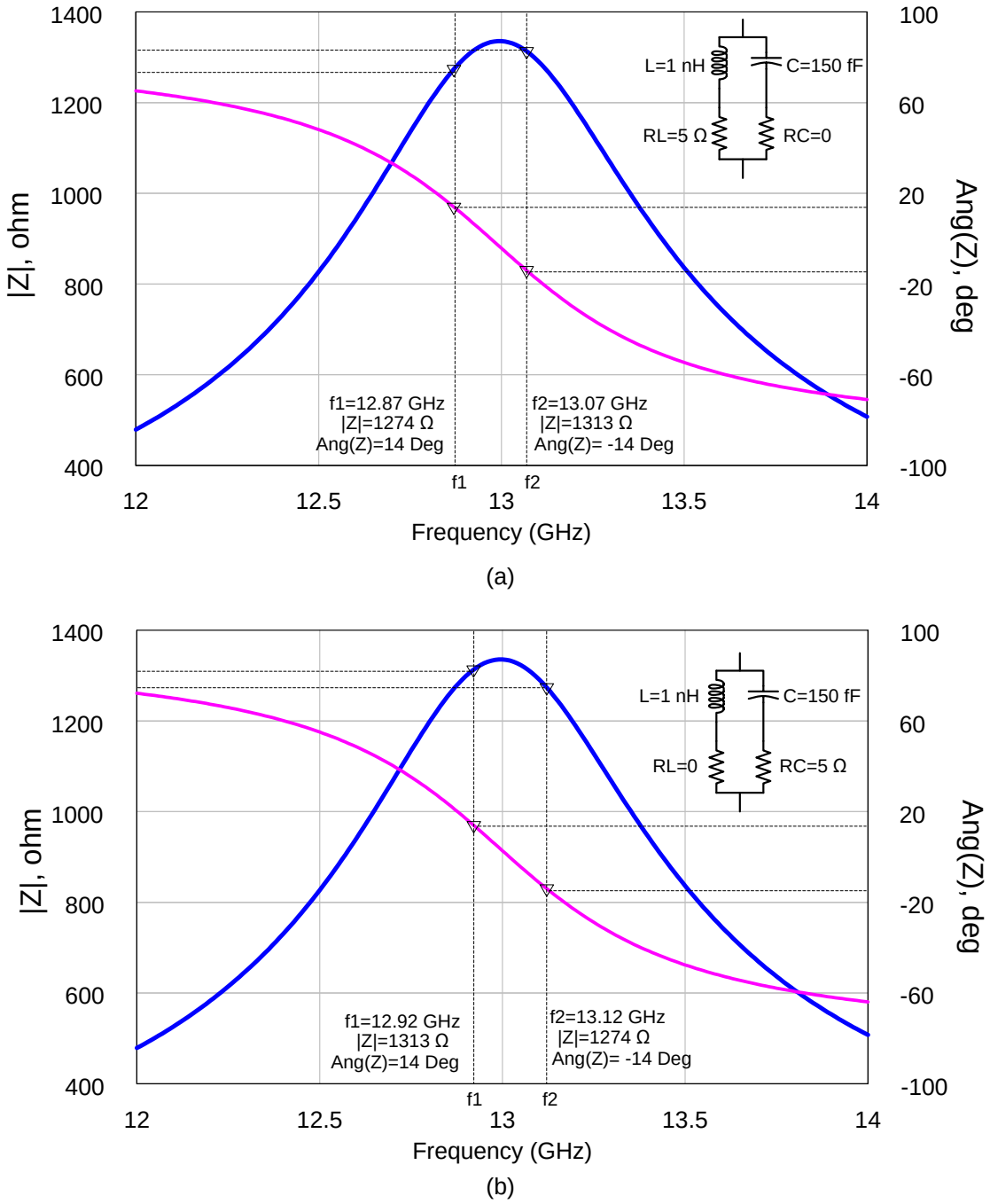


Figure 5.3. Magnitude and phase of the resonator impedance. (a) R_L>R_C, and (b) R_C>R_L.

If R_L>R_C, the magnitude of the LC tank impedance at f2 (where $\angle Z(j\omega) = -14^o$) is larger than that at f1 (where $\angle Z(j\omega) = 14^o$). On the contrary, if R_C>R_L, the magnitude at f1 is larger than that at f2. Since the feedback loop favors to reach a steady state with a

larger loop gain, it is mathematically proven in [83] that for $R_L > R_C$, the QVCO tends to oscillate at a frequency higher than the resonant frequency of the LC tank, and vice versa. In the case of a positive frequency shift, the tank is capacitive, and it is called the *capacitive mode*. Conversely, the tank is inductive for a negative frequency shift and it is called the *inductive mode*. For that reason, it is concluded that the QVCO oscillates in the capacitive mode for $R_L > R_C$ and in the inductive mode for $R_C > R_L$.

5.2.3 **Oscillation mode control**

Varactors are widely used in monolithic CMOS LC-based VCOs [84]-[86]. Using the aforementioned 13-GHz QVCO example with a generic schematic of Figure 5.1, a LC tank contains a 150 fF varactor in place of the capacitor and a 1 nH inductor of a quality factor of 16 at 13 GHz. The equivalent series resistance of the inductor is 5 ohm. As for the 150-fF varactor in Taiwan Semiconductor Manufacturing Company (TSMC) 90-nm CMOS, its capacitance and quality factor at various V_{TUNE} conditions are shown in Figure 5.4.

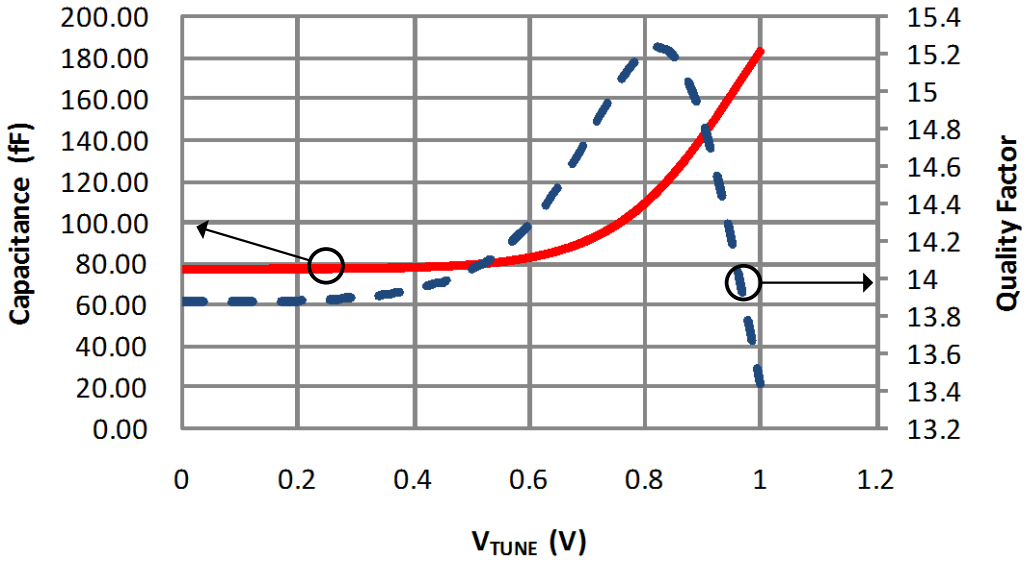


Figure 5.4. The capacitance (red solid line, left y-axis) and quality factor (blue dashed line, right y-axis) versus V_{TUNE} of the 150 fF varactor in TSMC 90-nm low power CMOS process.

When V_{TUNE}=1 V, the equivalent series resistance of the varactor (R_C) is 3 ohm. Since R_C<R_L, the QVCO tends to oscillate in the capacitive mode. When V_{TUNE}=0 V, R_C=12 ohm, therefore the QVCO tends to oscillate in the inductive mode. Simulations also indicate that QVCOs with bimodal oscillations typically experience pull-and-drag transient response between two modes during its startup [82]. Once the QVCO establishes stable oscillation in one mode, it maintains the positive feedback in this mode until a large external energy is applied to the system. Therefore, by means of setting the initial state of the varactor, the QVCO can be controlled to oscillate toward the desired mode. A control procedure example is described below for the QVCO to oscillate in the capacitive mode.

1. Before turning on Vdd, set V_{TUNE} to 1 V.

2. Turn on Vdd. The QVCO should oscillate in the capacitive mode.

3. Progressively decrease V_{TUNE} to obtain the desired frequency.

To set the QVCO to oscillate in the inductive mode, the difference is to set V_{TUNE}=0 V in Step 1. To obtain the desired frequency in the inductive mode, V_{TUNE} needs to be progressively increased.

5.2.4 **Experimental results**

A 13-GHz QVCO was fabricated in TSMC 90-nm CMOS process for the demonstration of a bimodal oscillation. The circuit schematic and die microphotograph are shown in Figure 5.1 and Figure 5.5, respectively.

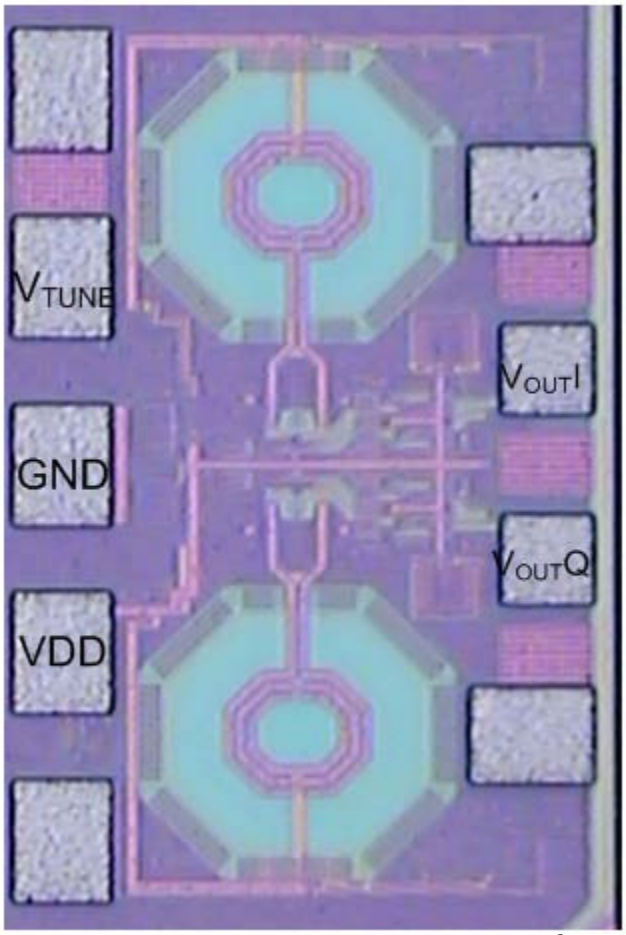


Figure 5.5. Die microphotograph of the QVCO. Chip area is 700x450 µm^2.

With 1 V supply voltage, the QVCO power consumption is 31 mW including source-follower buffers, which are not shown in Figure 5.1 for clarity. The measurement follows the three-step procedure. V_{TUNE} is set to 1 V, thus the varactor is reversed-biased during operations. After turning on the Vdd, the spectrum analyzer shows that the QVCO oscillates at 12.57 GHz. V_{TUNE} is then progressively decreased to obtain the frequency-tuning curve for the capacitive mode. Similar procedure with initially setting V_{TUNE} to be zero and then turning on the Vdd is operated again to obtain the inductive mode frequency-tuning curve. Both the capacitive and the inductive oscillation modes are successfully obtained by the proposed method of mode-control mechanism. Frequency tuning curves for both modes are shown in Figure 5.6. The two oscillation modes have a frequency offset of around 1 GHz between each other. The measured output spectra of both modes are shown in Figure 5.7 when V_{TUNE}=0.5 V. Figure 5.8 shows the measured phase noise versus offset carrier frequency, and the phase noise at 1-MHz offset frequency is -108 dBc/Hz.

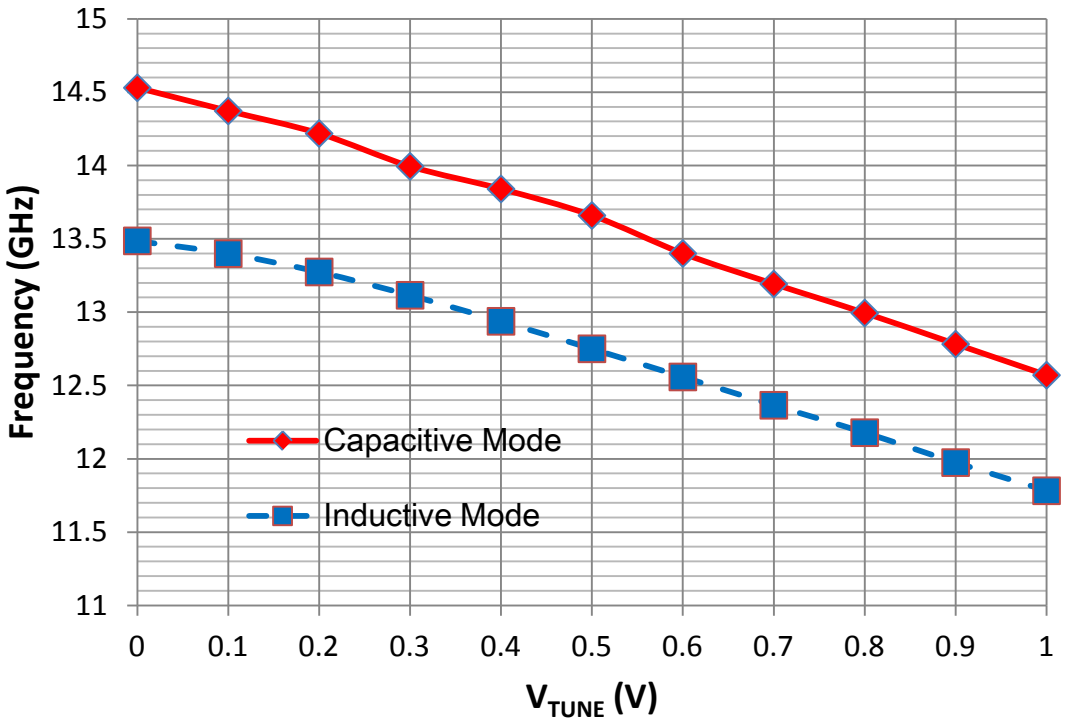


Figure 5.6. Output frequency versus V_{TUNE} for the capacitive mode (solid line) and the inductive mode (dashed line).

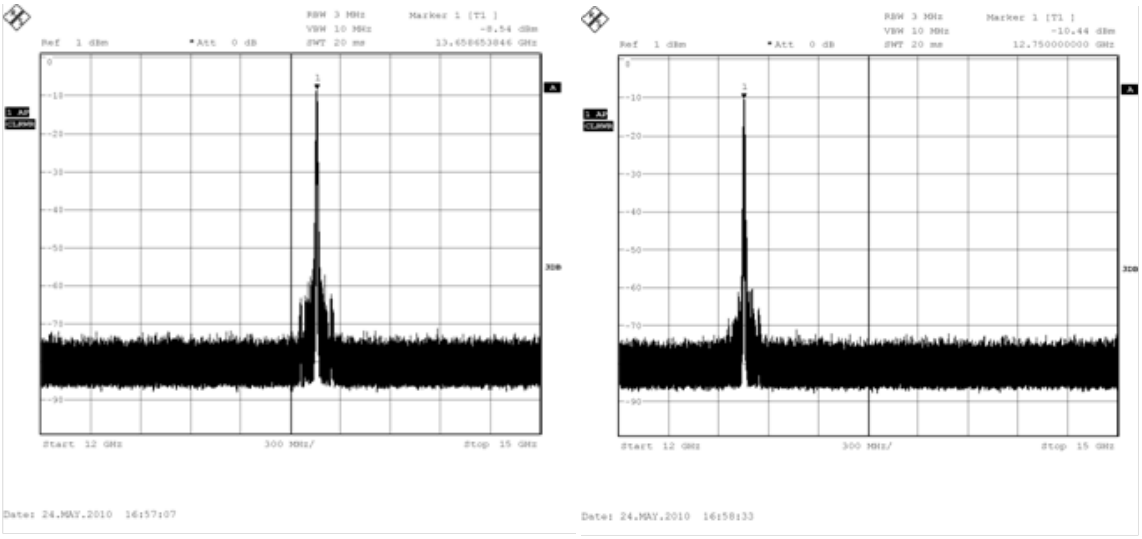


Figure 5.7. Measured spectra of bimodal oscillation in NMOS current-coupled QVCO. (a) Left: The capacitive mode. The QVCO oscillates at 13.659 GHz. (b) Right: The inductive mode. The QVCO oscillates at 12.75 GHz.

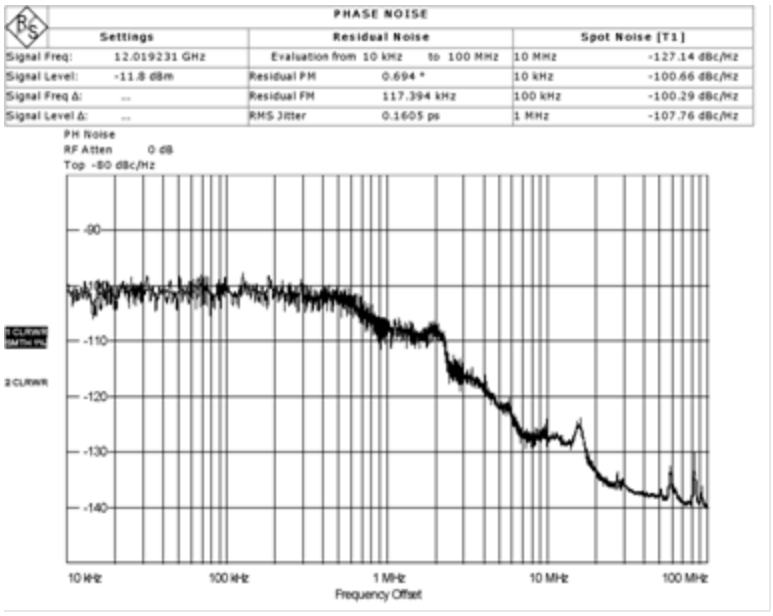


Figure 5.8. Measured phase noise of the QVCO shows -107.76 dBc/Hz at 1 MHz offset frequency.

5.2.5 **Summary**

The bimodal oscillation phenomenon inherent to LC-tuned QVCOs is analyzed and a systematic control methodology of the bimodal oscillation phenomenon is proposed for the current-coupled LC-QVCO topology. Both the capacitive mode and the inductive mode are successfully demonstrated by this procedure on a 13-GHz 90-nm CMOS QVCO experiment. By means of the proposed measurement procedure, the bimodal oscillation inherent to CMOS QVCOs can be observed and characterized. The bimodal oscillation phenomenon is no longer unpredictable in circuit implementation, thus ensuring a first-pass-success implementation of the targeted frequency synthesizer. Moreover, by manipulating the inherent bimodal oscillation phenomenon, both the capacitive mode and the inductive mode can be switched by controlling the initial condition. It is equivalent to provide a dual-frequency-tuning curve of the QVCO. The

dual-curve characteristic of the frequency tuning extends the frequency-tuning range without penalties on the phase noise.

5.3 Millimeter-Wave VCO Design

5.3.1 **Mm-wave VCO design considerations with respect to reliability**

CMOS Millimeter-wave VCO design techniques have been drawn lots of attention in the last decade [87]-[94]. Current state-of-the-art CMOS VCO targeting for highest frequency has achieved fundamental oscillation frequency higher than 200 GHz [92]-[94], which proves that stable oscillation sources for 60-GHz applications are feasible using standard CMOS technologies. However, for these mm-wave VCOs, one critical problem is the limited output power. These CMOS VCOs require power-hungry output buffers for a 50-Ω load, for testing or for mixer interface. Consider the practical case that the mm-wave VCO usually drives the mixer through a power distribution network, the loss of the network degrades the available power for the mixer and therefore more dc power has to be wasted on the buffer amplifiers to compensate the loss.

In order to increase the output power of the mm-wave VCO, a straightforward method is to increase the supply voltage. Higher supply voltage leads to larger voltage swing of the VCO and also increases the output power. Nevertheless, the trend of CMOS technology roadmap reveals a progressive reduction in threshold and supply voltage because of the digital circuit requirements as shown in Figure 5.9 [95]. Although advanced technology nodes provide higher intrinsic gain and less parasitic capacitance, which are both favored for the design of mm-wave VCOs, the decreasing voltage headroom further limits the output power of the mm-wave VCO. Under the limitation,

critical analyses with respect to the supply voltage for the device reliability when considering a higher bias are required.

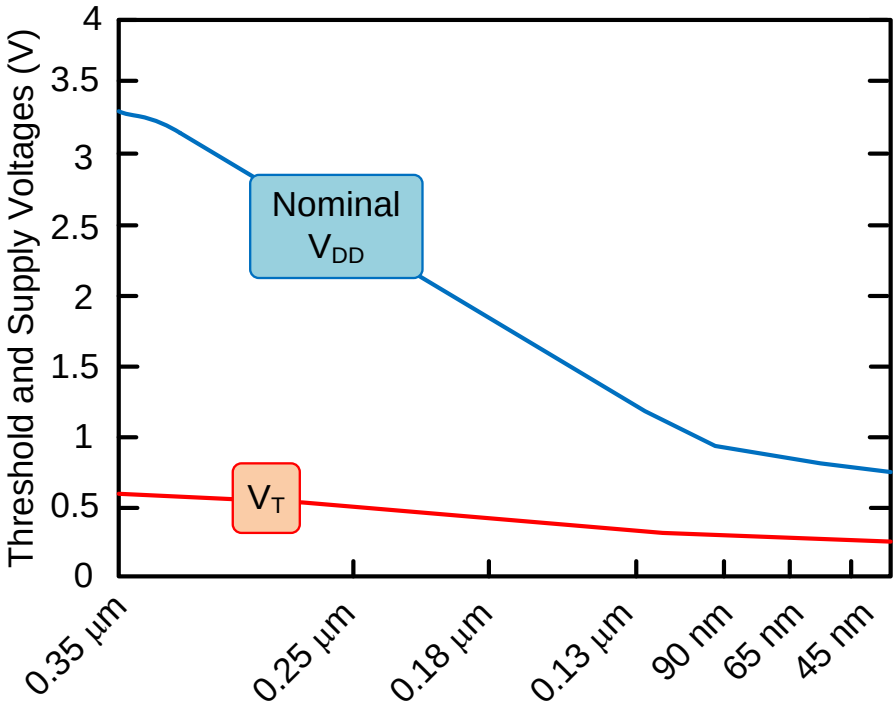


Figure 5.9. Threshold and supply voltage with respect to the CMOS technology roadmap [95].

A millimeter-wave VCO is designed for fundamental oscillation frequency at 42-48 GHz as shown in. The VCO has a LC tank resonates at the designed frequency, and the resonance frequency can be tuned by controlling the voltage of the varactor. The inductor is realized by TFMS. As mentioned in Section 3.2, transmission line characteristic can be well predicted and modeled, and therefore ensures the VCO oscillates at the correct frequency range. A cross-coupled NMOS pair generates negative resistance of $R_{CC}=-2/g_m$, where g_m is the transconductance of the NMOS FET [96]. NMOS FET size and bias current are designed to generate $|R_{CC}|$ that is less than or equal

to the equivalent parallel resistance of the tank. As a consequence, the loss of the LC tank is cancelled out by the cross-coupled pair negative resistance, and therefore ensures a steady oscillation.

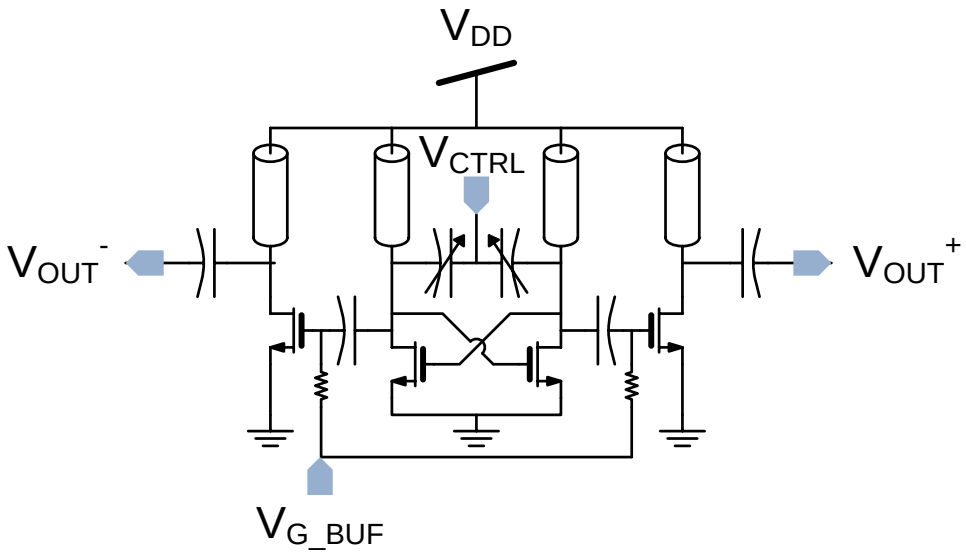


Figure 5.10. Schematic diagram of the mm-wave VCO.

When the VCO is in steady oscillation state, the two transistors of the cross-coupled pair switch on and off alternately, results in high voltage swings on these transistors. Theoretically, the swing can be higher than 2Vdd. For transistors that are exposed to voltage exceeding the standard Vdd, two effects dominantly degenerate the transistor lifetime: negative bias temperature instability (NBTI) and hot carrier injection (HCI). NBTI only subjects to PMOS devices. Since the mm-wave VCO only consists of NMOS devices, NBTI can be neglected. The hot carrier injection occurs when the NMOS device is exposed to a high drain-to-source voltage (V_{DS}) with a large drain current. Hot carriers are defined as the carriers with high kinetic energy. HCI effect is illustrated in Figure 5.11. Hot carriers accelerated toward the drain by a lateral electric field across the

channel lead to secondary carriers generated through impact ionization. Either the primary or secondary carriers can gain enough energy to be injected into the gate. This creates traps at the silicon substrate to gate dielectric interface, as well as dielectric bulk traps, and hence degrades device characteristics such as the threshold voltage. These "traps" are electrically active defects that capture carriers at energy levels within the bandgap. Examples of HCI degradation are a shift of V_T and a shorter gate-oxide-breakdown lifetime. Both are detrimental for the reliability of mm-wave VCOs.

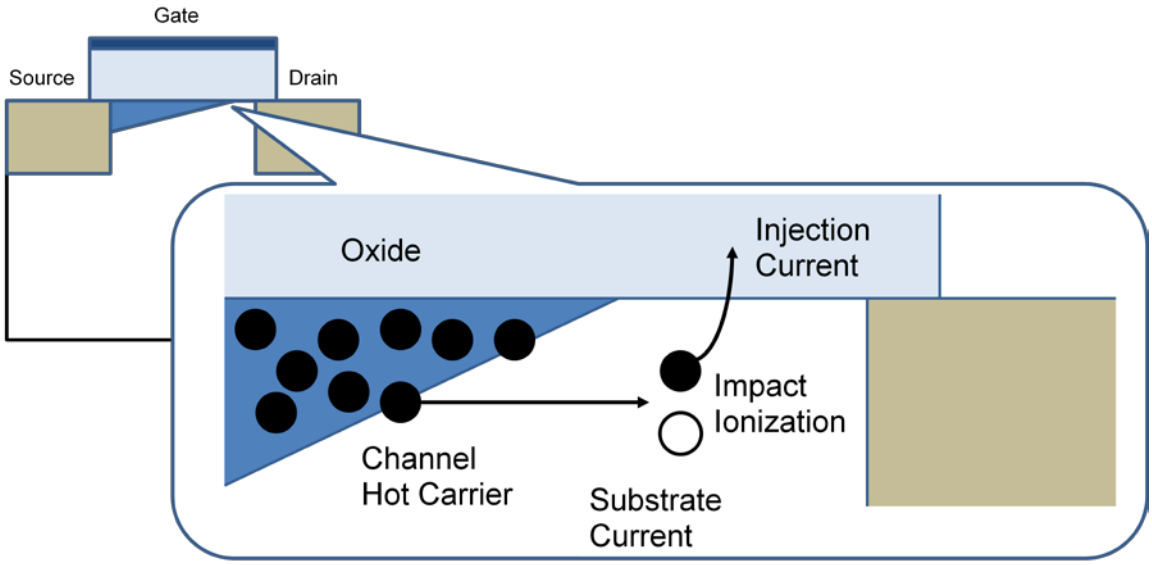


Figure 5.11. Graphical illustration of hot carrier injection (HCI) effect.

5.3.2 Mm-wave VCO performance characterization

The mm-wave VCO is implemented in a 65-nm CMOS process. The die microphotograph is shown in Figure 5.12. The chip is measured via on-wafer probing with the test setup illustrated in Figure 5.13. Output frequency and power is measured with a Rohde & Schwarz FSU50 spectrum analyzer and the measurement results are shown in Figure 5.14 and Figure 5.15. Two chips are measured and good repeatability is proven from the measurement results. With controlling the varactor tuning voltage

(V_{TUNE}) from 0 to 1.4 V, the mm-wave VCO is able to oscillate from 41.6 to 47.4 GHz. In this measurement, the VCO is biased at supply voltage of 0.9 V. Current consumption is 39 mA, where the core contributes 21 mA and the buffer contributes 18 mA.

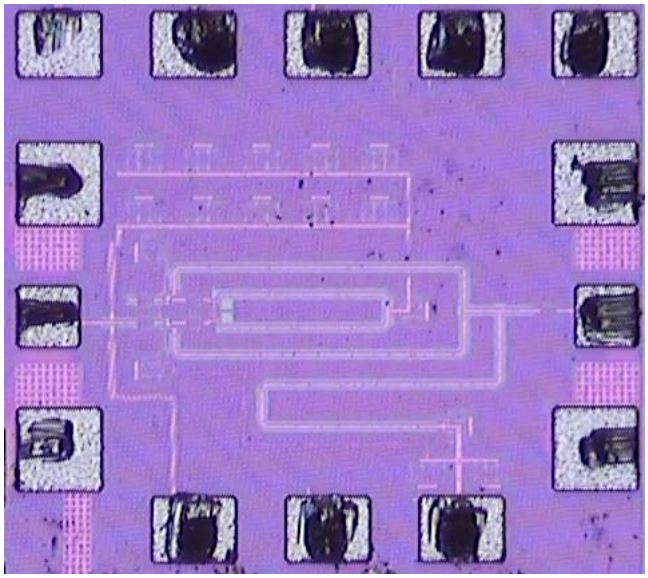


Figure 5.12. Die microphotograph of the mm-wave VCO

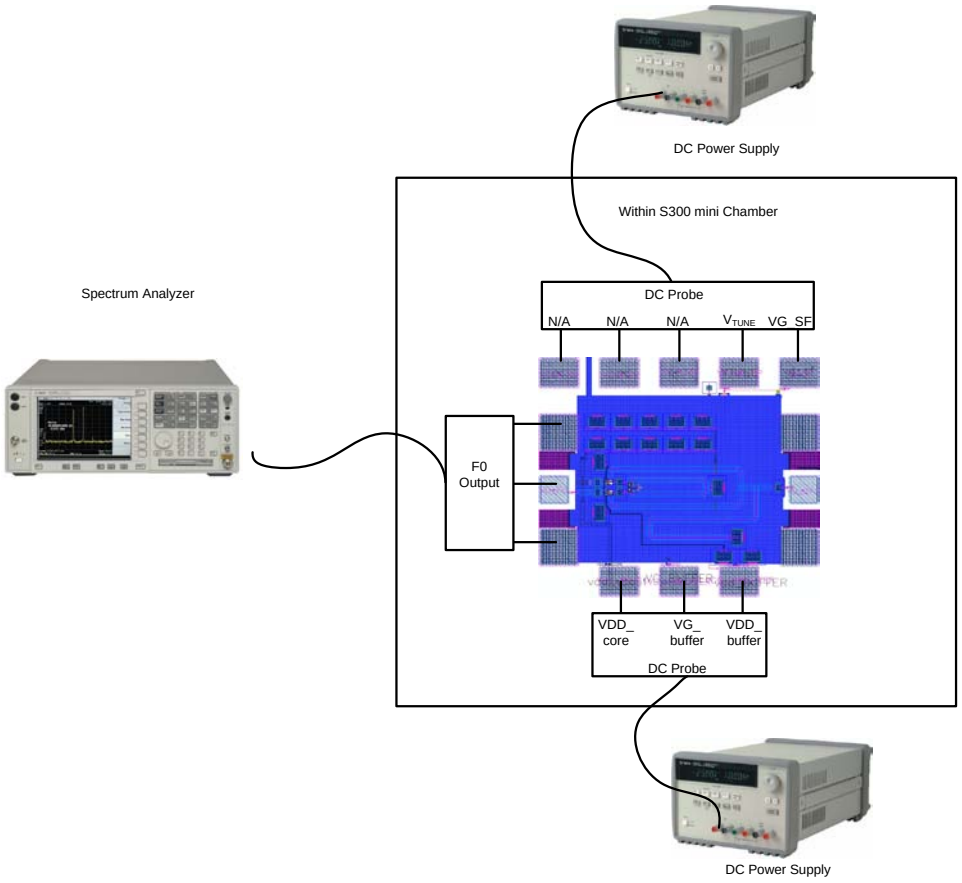


Figure 5.13. Measurement setup of the mm-wave VCO.

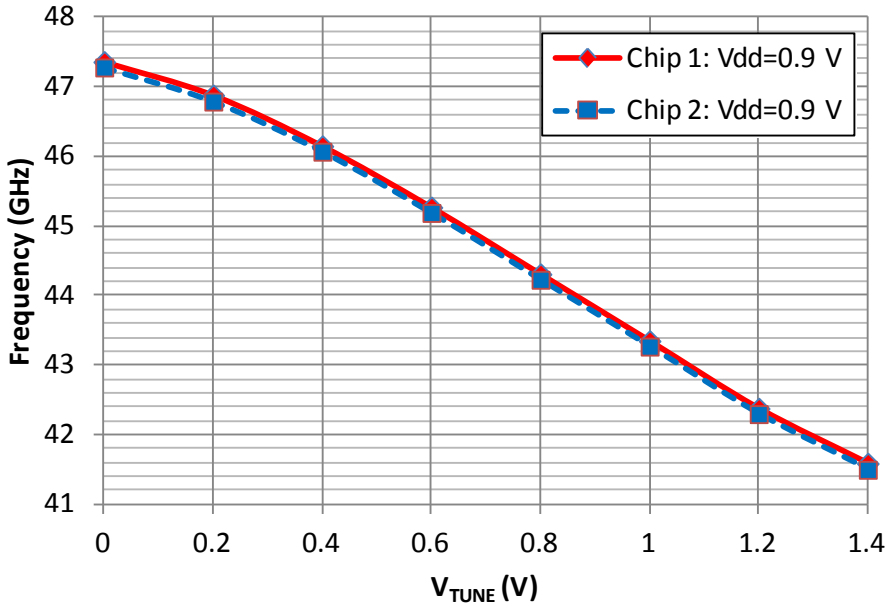


Figure 5.14. Mm-wave VCO output frequency versus V_{TUNE} for two chips.

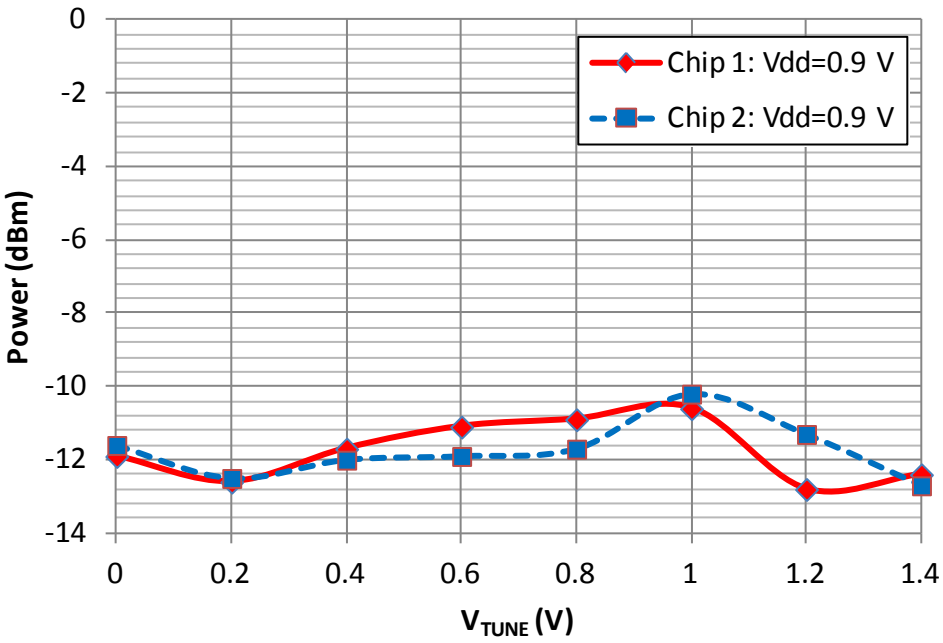


Figure 5.15. Mm-wave VCO output power versus V_{TUNE} for two chips.

The mm-wave VCO is also measured under different supply voltages. When V_{TUNE} is fixed at 0, Vdd from 0.6 to 1.6 V were tested with the output frequency and power plotted in Figure 5.16. Thanks to the differential topology, the output frequency is not sensitive to Vdd. Output power increases proportionally as Vdd increases from 0.6 to 1.6 V. The measurement results prove that increasing supply voltage is a straightforward but effective method to enhance VCO output power. Nevertheless, the standard Vdd of 65nm CMOS is 0.9 V, and HCI effect takes place at V_{ds}=V_{gs}=1.2 V. The performance is predicted to degrade with high voltage stress after a long time. Therefore, in the following experiment, the mm-wave VCO is biased with high Vdd for a long period for reliability characterizations.

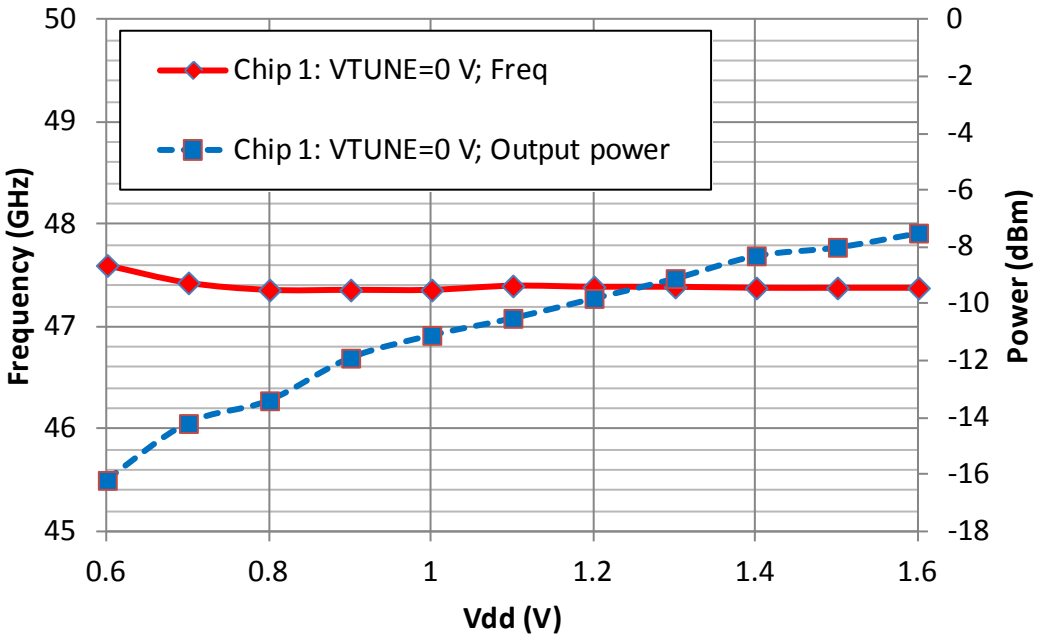


Figure 5.16. Mm-wave VCO output frequency and power versus supply voltage Vdd. Frequency is on the left vertical axis and power is on the right vertical axis.

When the VCO is biased at Vdd higher than 1.2 V, strong electric fields are generated inside the transistor and thus reduce the time at which the hot-carrier effects can be observed [97]. Performance degradation was measured for 48 hours of stress with power supply voltage set to 1.6 V. The stress voltage is lower than the one used in [98], which is 1.7 V, but still high enough to accelerate the hot-carrier effects for observable significant performance degradation. Because of the degradation of threshold voltage and mobility, which results in a reduction of transconductance, the mm-wave VCO output power decreases as observed in Figure 5.17. The frequency does not change. Phase noise is also measured in Figure 5.18, which records the best, the worst, and the average phase noise after five measurements for each stress time. However, because the VCO is not frequency-locked with a phase-locked loop, plus the VCO gain (KVCO) is as high as 4.1

GHz/V, frequency drift is severe. As a consequence, the phase noises measured at 1-MHz offset has around 5 dB variations for each test under the same amount of stress time.

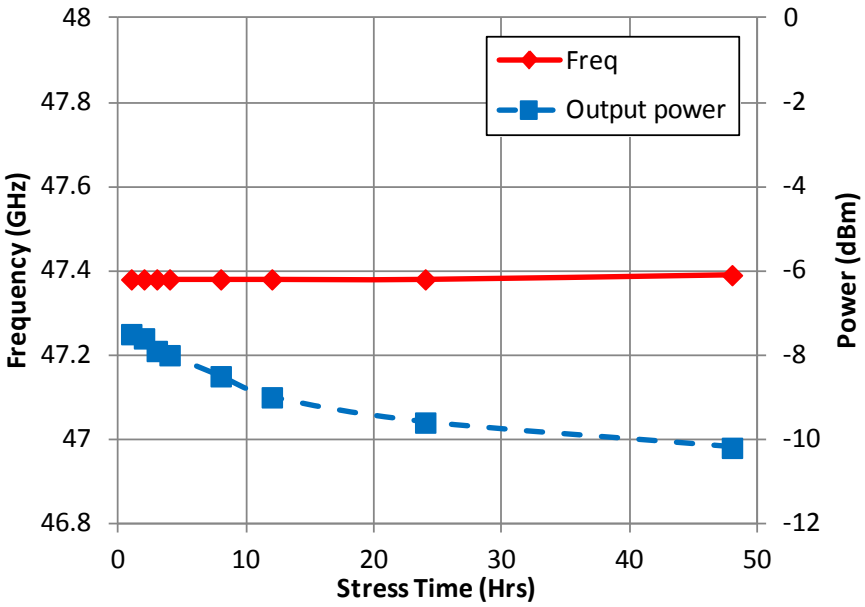


Figure 5.17. Mm-wave VCO output frequency and power versus stress time up to 48 hours. Frequency is on the left vertical axis and power is on the right vertical axis.

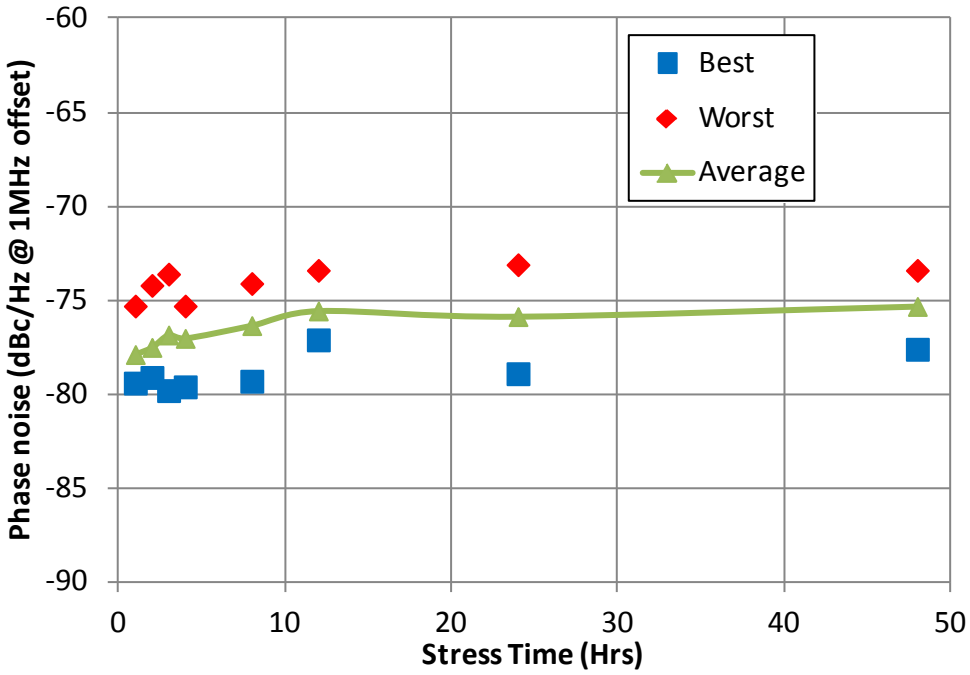


Figure 5.18. Mm-wave VCO phase noise measured at 1-MHz offset versus stress time up to 48 hours.

There were some literatures about the hot-carrier stress effects on low-frequency CMOS oscillators [99]. HCI effects on mm-wave power amplifiers were also published [97]-[98]. This experiment, to the best of the author's knowledge, is the first DC stress test on a millimeter-wave CMOS VCO. As predicted by [97]-[98], transconductance degradation caused by HCI effect degrades the RF performance at millimeter-wave frequencies significantly. In this experiment, the output power decreases 2.7 dB after 48-hours 1.6-V stress. With the reduction of output power, the phase noise should degrade correspondingly [72]. Nevertheless, because of the measurement limitations, we are unable to provide a phase-locked loop to mitigate the frequency drift caused by high KVCO. Therefore, in this experiment, the phase noise degradation is not able to be observed with high variation on the measurement results.

5.3.3 **Integrated VCO-mixer down converter codesign**

In Section 5.3.1 and 5.3.2, it is investigated that the reliability of the mm-wave VCO under high supply-voltage stress. The reason of increasing the supply voltage is to provide higher output power to drive the mixer. In the mm-wave transceiver SoC implementation, the mm-wave VCO is usually integrated with the PLL. Therefore, the VCO is usually placed away from the mixer in the floor plan. This arrangement results in the requirement of high power consumption on the local oscillator (LO) signal distribution network, which consists of a chain of mm-wave LO amplifiers. In this section, a new concept of integrating the mm-wave VCO together with the mixer is proposed. By driving the mixer closely to the mm-wave VCO in the physical layout, larger LO signal swing can be loaded on the mixer, which provides sufficient power for

optimized mixer conversion gain. Moreover, the topology neglects the need of the power-hungry LO amplifiers and enables low-power architecture of mm-wave receiver front end.

Figure 5.19 illustrates the functional diagram of the integrated VCO-mixer down converter, which is in the green rectangle. In this integrated down converter, millimeter-wave cross-coupled VCO (CC-VCO) investigated in the previous section is used as the LO frequency source (Figure 5.10). The receiver down-conversion mixer, which is shown in inset (a) of Figure 5.19, is designed using double-balanced Gilbert-cell topology. Double-balanced topology minimizes the LO leakage. One of the differential inputs is shorted to ground so that the mixer operates with a single-ended input from the output of the LNA. Small LO device sizes are chosen to minimize the loading effect on the VCO. The mixer has a bandpass inductive loading optimized for 13-GHz IF. The input of the mixer is matched to 50 Ω at 61 GHz by TFMS. A buffer is integrated at the output of the mixer for 50–Ω measurement system. The transistor level schematic diagram of the 50-Ω buffer is shown in inset (b) of Figure 5.19.

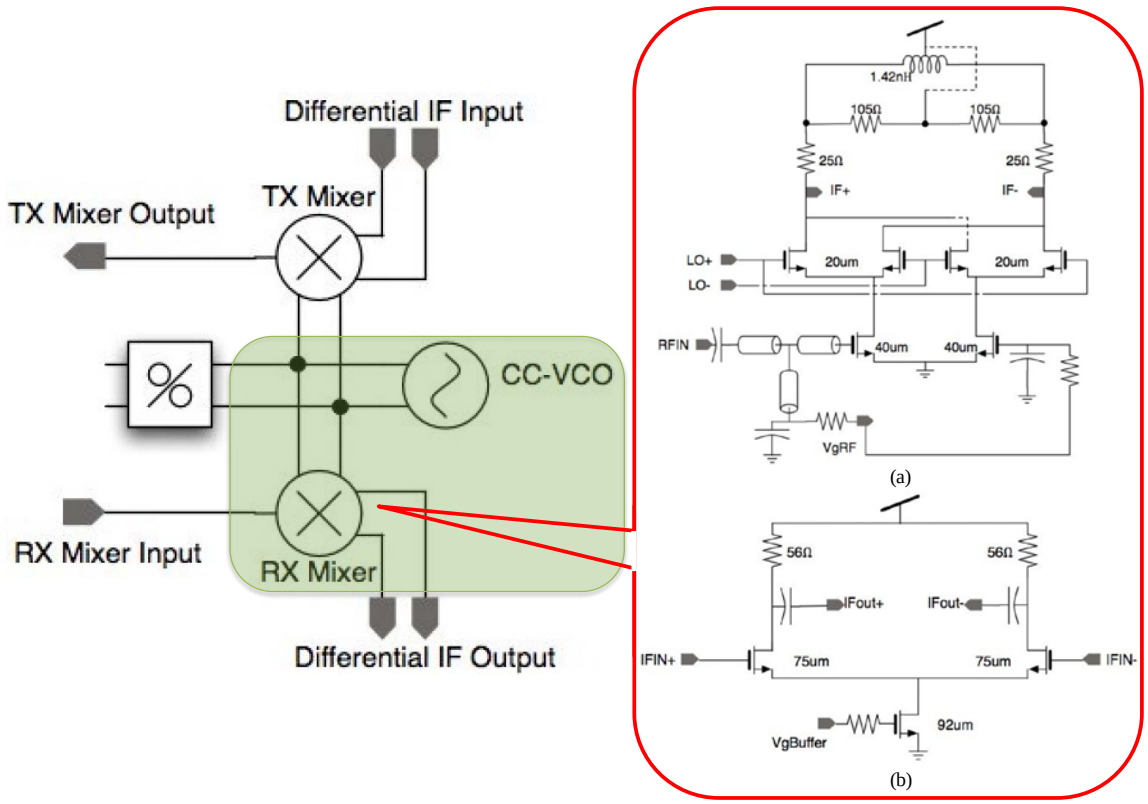


Figure 5.19. The functional diagram of the integrated VCO-mixer down converter, including a CC-VCO and a mixer consisted of a double-balanced Gilbert cell (inset (a)) and an output buffer (inset (b)).

5.3.4 VCO-mixer measurement results

The layout view and die microphotograph of the integrated VCO mixer is shown in Figure 5.20. The down-conversion mixer is tested with the LO fed internally by the mm-wave VCO. The RF signal is generated by a microwave signal generator, Anritsu MG3696B. The LO frequency is fixed at 47.4 GHz by setting V_{TUNE} of the mm-wave VCO to 0 V. In order to get a better performance, the supply voltage of the VCO is set to 1.1 V, which provides -10.5-dBm output power to the mixer from the measurement results given by Figure 5.16. Figure 5.21 shows the conversion gain of the mixer at fixed LO. The best conversion loss is 1.4 dB at 62-GHz RF input and 14.6-GHz IF output. At this frequency set, we also measured the conversion loss with RF input power sweep. The

RF linearity performance of the mixer, which is shown in Figure 5.21 as well, measures an input P_{1dB} of -7.5 dBm. The VCO-mixer down converter features low-power consumption by neglecting the power-consuming LO buffer amplifier chain. The mixer consumes 20 mA at 1.1 V supply voltage including 12 mA dissipated by the 50-Ω output buffer. The 50-Ω output buffer is for measurement purposes since the spectrum analyzer has a 50-Ω input. In the practical case, the buffer can be removed and therefore the total power consumption can be further reduced.

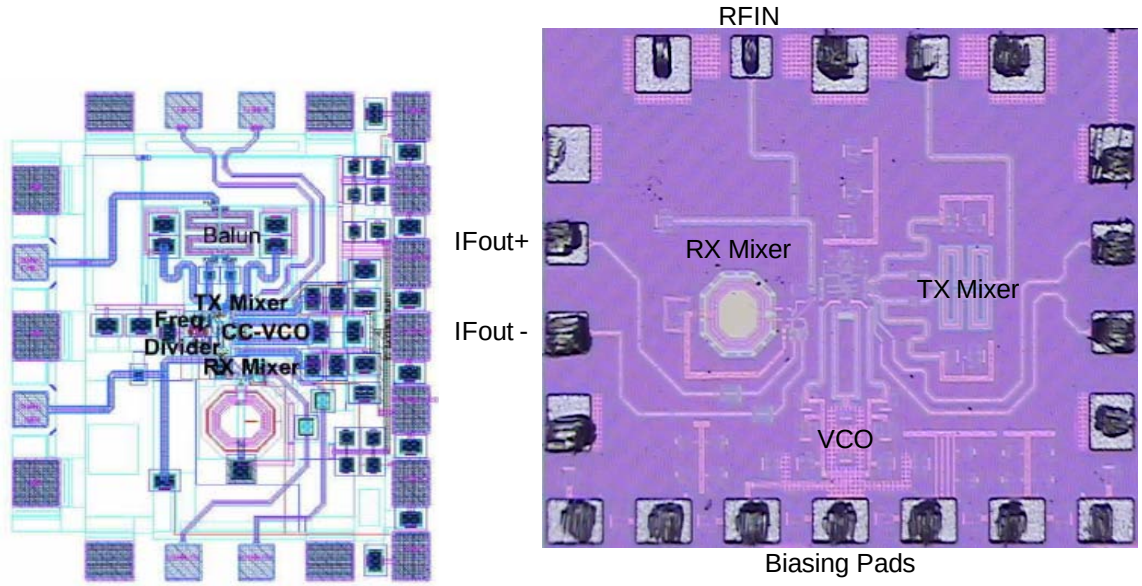


Figure 5.20. The layout view (left) and die microphotograph (right) of the integrated VCO mixer.

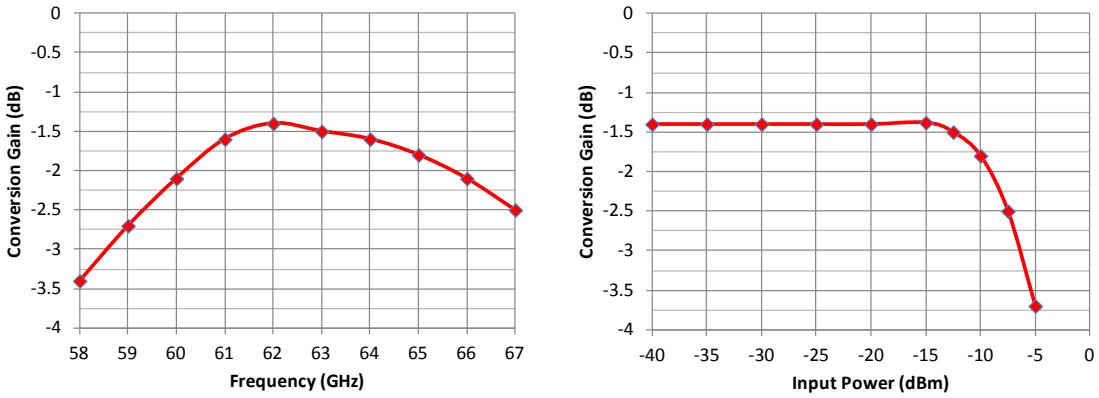


Figure 5.21. Measured conversion gain versus RF frequency sweep (left) and input power sweep (right).

5.4 Summary

This chapter summarizes the frequency generation circuits used in a super-heterodyne millimeter-wave receiver front end. Firstly, an IF QVCO is designed and fabricated. The bimodal oscillation phenomenon inherent to LC-tuned QVCOs is analyzed and a systematic control methodology of the bimodal oscillation phenomenon is proposed for the current-coupled LC-QVCO topology. By utilizing the dual tuning curve characteristic given by the bimodal oscillation the frequency-tuning range can be extended without penalties on the phase noise. The performances of the IF QVCO are summarized in Table 5.1.

Table 5.1. Performance summary of the QVCO.

Specification	Parameter	Unit
Technology	90	nm
Frequency	11.7 – 14.5	GHz
Tuning Range	21.4	%
Phase Noise @ 1-MHz offset	-107.8	dBc/Hz
Core Power Consumption	10.6	mW

Millimeter-wave frequency source, as the second part of this chapter, is designed and fabricated. A complete characterization on an mm-wave cross-coupled VCO is performed against voltage stress. The performance degradations caused by HCI effects are quantified. This mm-wave VCO is further integrated into an mm-wave down converter. With a proper design for the interface between the VCO and the mixer, the power consuming LO buffer amplifier chain is neglected, while proper RF performances are obtained as tabulated in Table 5.2.

Table 5.2. Performances summary of the integrated frequency down converter including the mmW VCO and RX mixer.

Specification		Parameter	Unit
Technology		65	nm
Supply Voltage		1.1	V
MmW VCO Frequency		41.6 – 47.4	GHz
MmW VCO Tuning Range		13	%
MmW VCO Output Power		-10.5	dBm
MmW VCO Phase Noise @ 1-MHz offset		≅ -75	dBc/Hz
Mixer Conversion Loss		1.4	dB
Mixer 1-dB IF Bandwidth		12.1 – 19.4	GHz
Mixer RF input P_{1dB}		-7.5	dBm
Power Consumption	MmW VCO	52.5	mW
	Mixer	20 (Gilbert cell: 8; 50-Ω buffer: 12)	

CHAPTER 6: POWER MANAGEMENT SYSTEM DESIGN

6.1 Introduction

Compared to other candidate standards for ultra-high data rate file transfer or video streaming applications such as 802.11.n (600 Mb/s), WHDI (1.5 Gb/s), and UWB (480 Mb/s), the aforementioned 60-GHz standards including IEEE 802.15.3c, IEEE 802.11.ad, and ECMA 387 provide not only a significant improved data throughput, but also another critical factor for system integration: less external components. It is due to the physical size of mm-wave antennae that antennae are small enough to be integrated in the package [100] or even on the chip [101] for the first time in the history of radio development. Furthermore, for short-range indoor data transfer or video streaming applications, the required output power can be sufficiently provided by a typical on-chip CMOS mm-wave PA [68]-[69]. Thus, the external PA, which is usually used in the wireless local area network (WLAN) systems, can be removed. Therefore, the 60-GHz radio can be integrated as an all-in-one solution with low rest-of-bill-of-materials (RBOM) cost. This advantage provides strength for the 60-GHz radio in the competition from a system integrator's perspective. However, recent 60-GHz transceivers haven't considered the integration of the power management circuitry. Most of these 60-GHz transceivers require multiple supply voltages for different circuit blocks for performance optimization. For example, the PA requires higher supply voltage for boost to the output power [102]. The VCO within the frequency synthesizer sometimes uses a lower supply voltage for better long-term yield [60]. Some mm-wave frequency synthesizers even use different supply voltages for the VCO and the charge-pump circuit for wider frequency-tuning

range. Moreover, as a basic guideline, the supply voltages of the analog and the digital circuits should be separated. These requirements indicate that multiple linear regulators or dc-dc converters are necessary for system integration. Nevertheless, the form factor and the cost of RBOM increase to satisfy the power management requirements as well.

The solution of this problem is to integrate the power management circuitry in the 60-GHz transceiver SoC. Low-dropout (LDO) regulators are favored for RF applications because of its low-noise output. Several publications [103]-[104] discussed the CMOS LDOs designed for RF transceiver, which emphasizes on the low frequency, commercialized standards. However, for an mm-wave transceiver, the LDO specifications are different from the LDO specifications for low frequency RF systems. Therefore, a dedicated LDO system for the 60-GHz radio is necessary. In this chapter, firstly, the design considerations of the LDO used in the 60-GHz radio receiver are discussed. With these design considerations, a power management system based on LDOs for 60-GHz radio is designed, fabricated, and tested.

6.2 LDO System Design Considerations for 60-GHz Radio

Current CMOS frequency synthesizers designed for 60-GHz radio reveal worse phase noise performances compared to those low-frequency RF counterparts. Recent publications reveal phase-noise performances around -80 dBc/Hz at 1 MHz offset for frequency synthesizers operating directly at mm-wave frequencies [105]-[107]. Frequency multipliers, such as doublers or triplers, enable the use of low-frequency synthesizers [108]-[109]. Nevertheless, the phase-noise performance still suffers from a penalty of $20\log_{10}N$, where N equals to two and three for frequency doublers and triplers, respectively. As a result, by adding on the 6 and 9.5 dB penalties for frequency doubler

and tripler, the phase noises are still around -80 dBc/Hz at 1 MHz offset. This phase-noise performance barely satisfies the requirement of basic non-constant envelope modulation schemes. Therefore, low-noise performance is an important specification of the LDO because there is no margin for further phase noise degradation caused by supply noise injection. Moreover, it is better to perform a direct co-simulation of the LDO and the VCO, which gives the RF and analog designers more information regarding the system integration.

For mm-wave circuits, the ac-decoupling capacitor is less than 1 pF for each ac-ground node. Although additional ac-decoupling capacitors are employed along the power line inside the chip, the overall capacitances are still much less than that in the low frequency RF transceiver counterparts. Furthermore, no additional off-chip ac-decoupling capacitor is required for supply noise filtering. Therefore, the load capacitance of the LDO used in 60-GHz radio is around several nano-Farad. This is quite different to those conventional LDO designs, which possesses several micro-Farad capacitive loads. The extremely low equivalent series resistances (ESRs) for on-chip metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors are another significant difference to conventional LDO designs. These major differences cause serious loop-stability issue for this dedicated LDO design for 60-GHz radio and a careful allocation of the poles and zeros of the LDO is needed.

The Georgia electronic design center (GEDC) 90-nm CMOS 60-GHz radio has two supply voltages for analog and digital power supplies. The analog supply voltage of 1.2 V is for the RF transmitter and the receiver front end, the IF circuit, and the analog baseband circuit. The digital supply voltage of 1 V is for the digital baseband circuit and

serial peripheral interface (SPI). The power management system diagram is shown Figure 6.1.

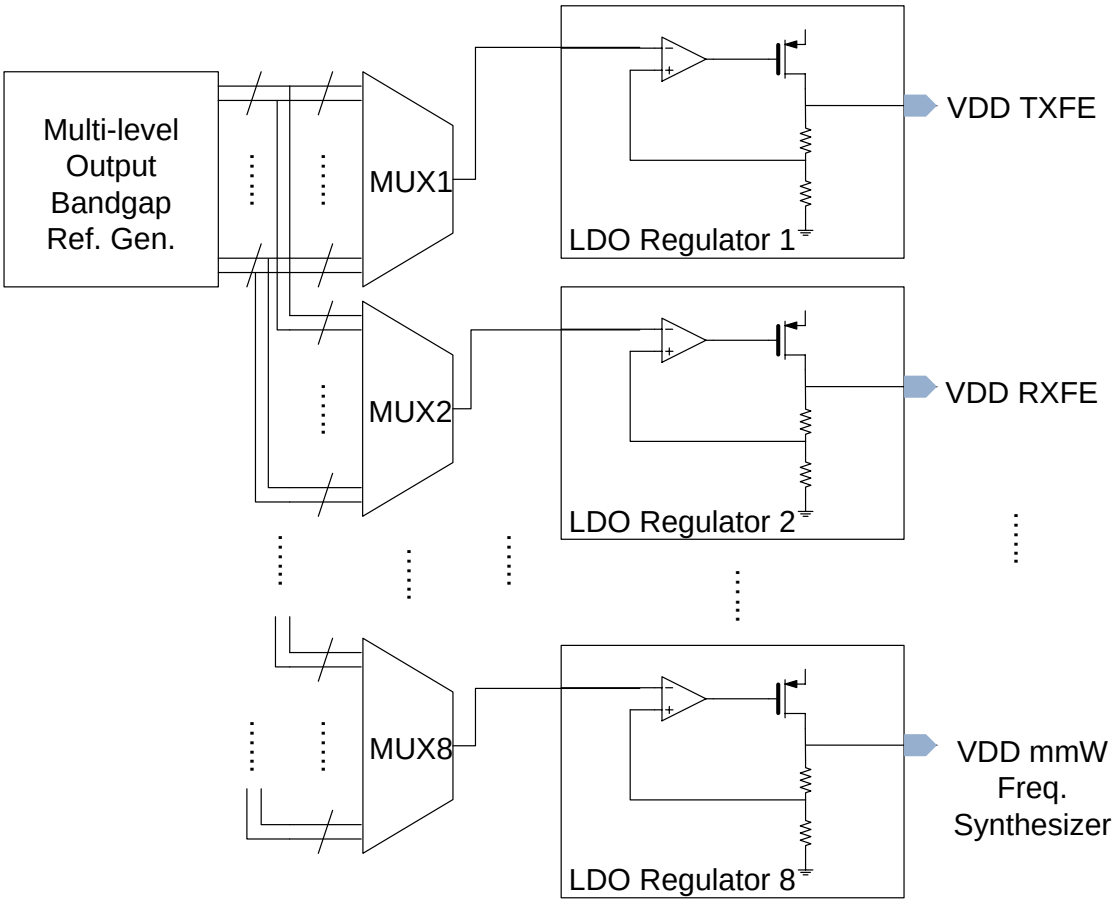


Figure 6.1. The block diagram of the power management system.

The power management system consists of eight LDOs. Four LDOs are located at the transmitter side while the other four LDOs are located at the receiver side with reference voltages coming from multilevel bandgap-reference-voltage generators. The power management system is embedded in the GEDC 60-GHz transceiver SoC implemented in a standard 1-poly-7-metal (1P7M) 90-nm CMOS technology. Thick

oxide devices, which are able to sustain a maximum voltage of 3.3 V, are used for all the building blocks because of reliability considerations.

6.3 Building Blocks Design of the 60-GHz Radio Power Management System

6.3.1 Bandgap reference voltage generator

The multilevel-output bandgap reference voltage generator provides multilevel dc outputs from 0.95 to 1.25 V. The dc outputs are temperature compensated. It is optimized to be insensitive to process corners and supply voltage variations. The circuit schematic diagram is shown in Figure 6.2.

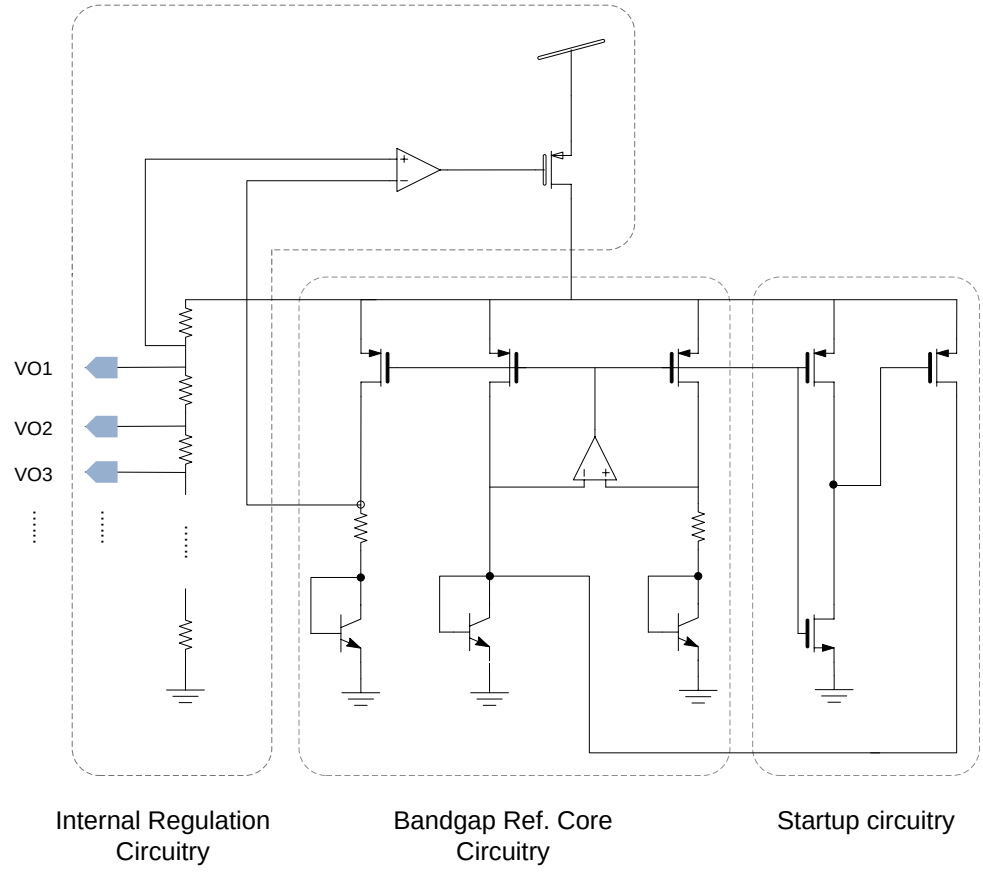


Figure 6.2. The schematic diagram of the multilevel bandgap reference voltage generator.

The circuit can be divided into three parts: the bandgap reference core circuitry, the internal regulation circuitry, and the startup circuitry. The bandgap reference core circuit is a classic 1.25-V bandgap reference voltage generator. NPN bipolar junction transistors (BJTs) are used because the NPN BJTs have higher current gains (β) than the PNP BJTs. Since the supply voltage of the power management units may vary from 1.8 to 3.3 volts, it is unable to keep a temperature invariant dc output within such a wide range supply voltages for the bandgap reference core itself, especially in a standard bulk CMOS technology, in which the β of the parasitic BJT is usually lower than ten. To solve this problem, an internal regulation circuitry is used in the multilevel output bandgap reference generator. It provides an internal regulated supply voltage of 1.5 V for the bandgap reference core under different external supply voltages, which may vary from 1.6 to 3.3 V. Furthermore, the virtual-short characteristic of the regulation amplifier provides a buffered output for the bandgap reference core. Therefore, a resistive divider can be used to obtain multilevel temperature-invariant dc outputs without affecting the internal mechanism of the bandgap reference core.

6.3.2 **LDO regulator**

LDO regulator is a feedback system that maintains the output dc level under different input voltages and load currents. The schematic diagram of the LDO regulator is shown in Figure 6.3.

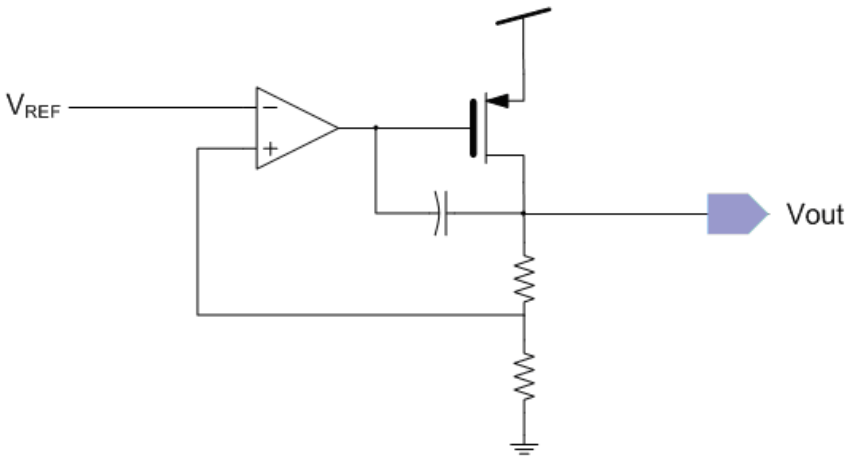


Figure 6.3. The schematic diagram of the LDO regulator.

The LDO regulator uses a single stage error amplifier, and therefore the overall system has only two poles at low frequency. Conventional LDO regulators use a two-stage opamp as the error amplifiers and therefore the overall system has three poles at low frequency. An additional compensation network is necessary for stability concern. A miller compensation capacitor is added on the power transistor. This gives the LDO a dominant pole at low frequency no matter how the loading capacitance changes. The stability can be ensured under a very wide range of the decouping capacitance from a few pico-Farad to tens of nano-Farad. The miller compensation capacitor is realized by a metal-oxide-semiconductor capacitor (MOSCAP) with high capacitance density. Although the terminal dc voltages may affect the capacitance of the MOSCAP, it has been taken into consideration to ensure reasonable phase margin of the feedback loop. A 60-dB gain folded-cascode operational amplifier is used in the feedback loop.

6.4 Measurement Results and Summary

The linear regulator array is integrated in the 60 GHz transceiver. Figure 6.4 shows the die photo with the linear regulator array located at the top and the bottom of the chip.

Both the regulator arrays at the top and the bottom consist of a multilevel bandgap reference voltage generator and four LDOs. The external power supplies are fed into the chip by the edge pads at the top and bottom of the chip. The internal pads that are in parallel to the edge pads are for testing purposes. Standalone measurement result for the regulator array is obtained from these pads. The quiescent current of the regulator array is 620 μA under 1.6 to 3.3 V supply voltages. As shown in Figure 6.5, the line and load regulation measurement results are measured for 1.2 V output; LDO output voltages for the supply voltage varying from 1.6 to 3.3 V and load current varying from 0 to 200 mA are tested.

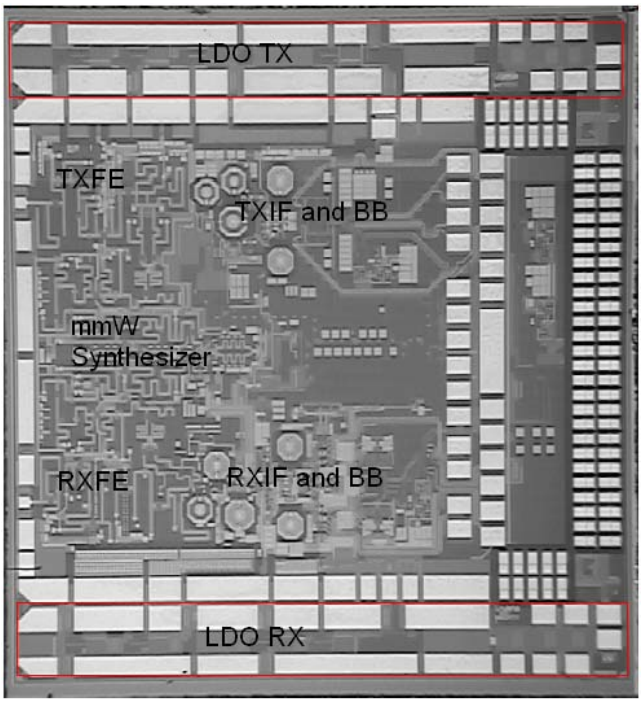


Figure 6.4. Die microphotograph of the 60 GHz radio SoC. The linear regulator arrays are marked in red circles at the top and the bottom of the chip.

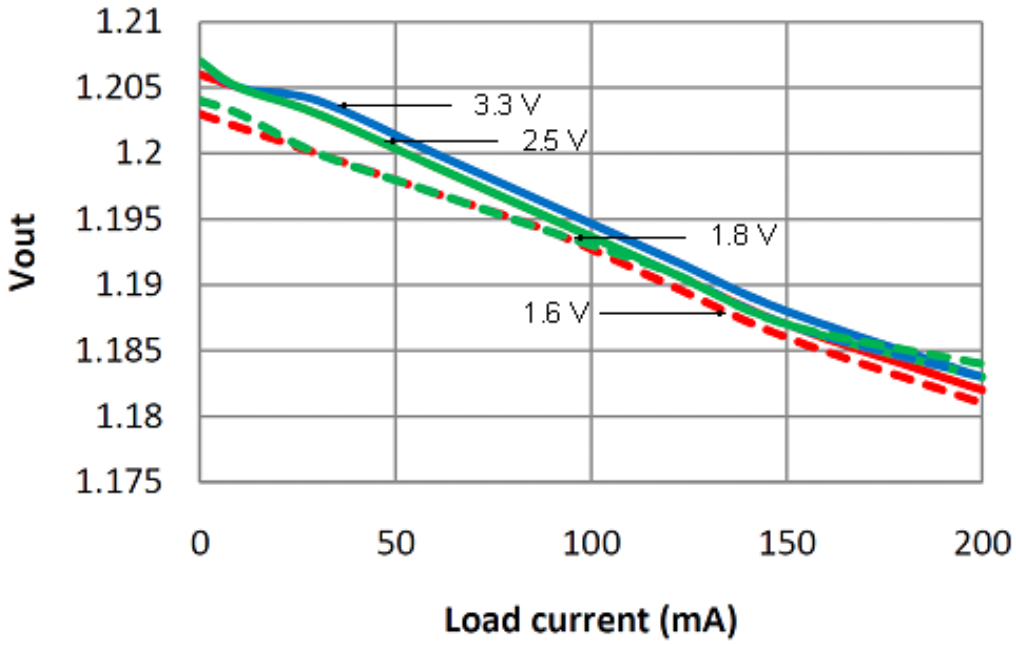


Figure 6.5. Line and load regulation of the linear regulator.

Figure 6.6 shows the LDO output voltage versus temperature at zero-load-current condition.

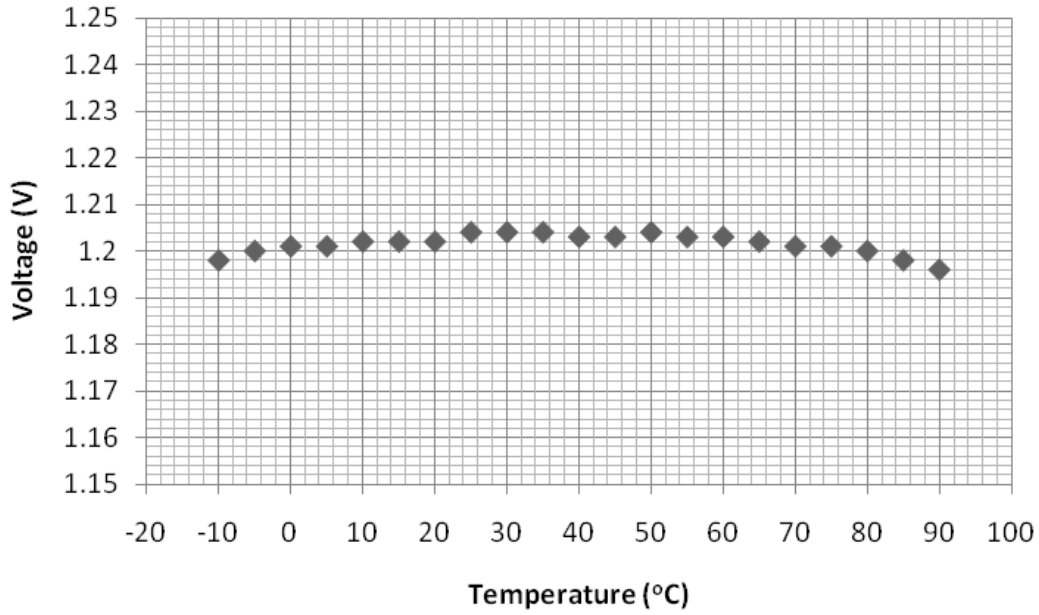
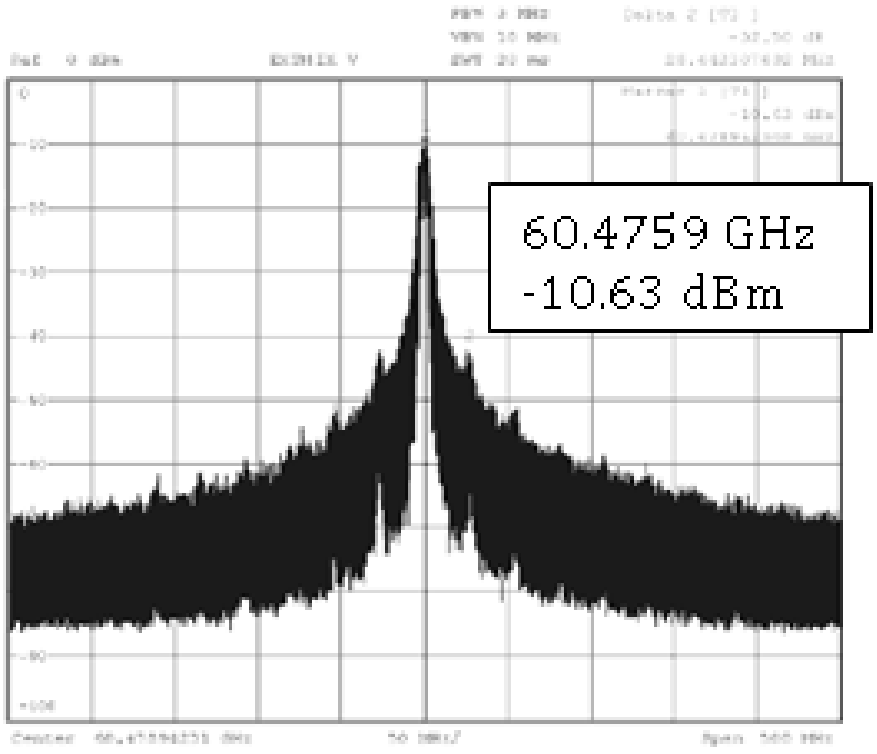


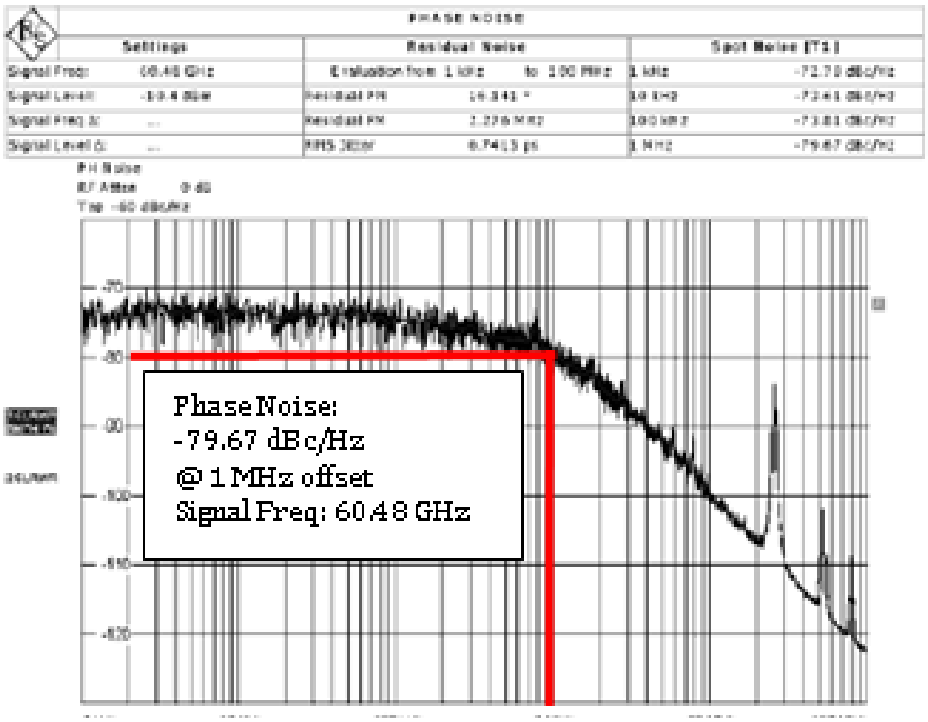
Figure 6.6. LDO output voltage with respect to temperature variation.

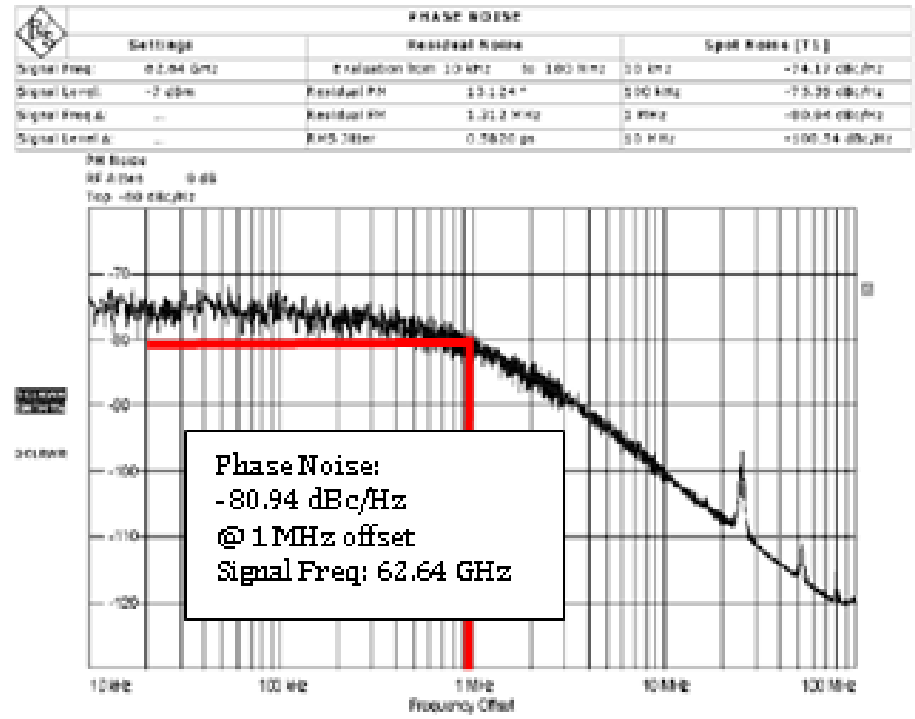
The output voltage variation for different input voltages and load currents is within 25 mV. To test the noise performance of the regulator array, the regulator is used to feed the supply voltage of the transmitter. When no modulated signal was fed, the output spectrum and phase noise of the transmitter are measured for channel 2 (60.48 GHz) and 3 (62.64 GHz) as shown in Figure 6.7.



(a)

Figure 6.7. (a) Transmitter output spectrum for channel 2 (60.48 GHz), and (b) phase noise plots for channel 2 (60.48 GHz) and channel 3 (62.64 GHz).





(b)

Figure 6.7. Continued.

The phase noises are -79.7 and -80.9 dBc/Hz at 1 MHz offset. The measurements results prove that the feasibility of integrating the linear regulator within an mmW transceiver without performance degradation. Comparing to the transmitter phase noise measurement results with noise-free battery as the voltage supply, the phase noise degrades 1-2 dB at 1-MHz offset. The measurement performance is summarized in Table 6.1. In conclusion, in this chapter, a design methodology for power management system dedicated for 60-GHz mmW transceiver is introduced. The system is integrated in a 60-GHz transceiver SoC and used to provide the supply voltage of the SoC. The results prove that the SoC functions normally with a marginal degradation on the noise performance.

Table 6.1. Performance summary of the power management system.

Specification	Parameter	Unit
Temperature Variation	<10	mV
Line Regulation	1.192 – 1.195 (@100 mA load current)	V
Load Regulation	1.184-1.204 (@ 1.8 V input voltage)	V
Quiescent Current	620	μA
PSRR	55 (@ 1kHz) 10 (@1 MHz)	dB
Minimum Dropout Voltage	290	mV
Maximum Output Current	200	mA
Phase Noise Degradation when used in a 60-GHz Tx (Compared to Battery)	1 -2	dB

CHAPTER 7: CONCLUSIONS

The final chapter concludes the research in developing key components for manufacturable and low-power CMOS millimeter-wave receiver front end. Technical contributions of this research work are presented in Section 7.1. Potential research directions for future development related to this work are also discussed in Section 7.2.

7.1 Technical Contributions

This dissertation investigates the designs of key components in a CMOS millimeter-wave receiver front end. This research drew lots of attention since the 60-GHz band spectrum released by FCC in 2001 [1]. Ten years passed, lots of research literatures have been published, and some of them became products for wireless video streaming [4]. Nevertheless, nowadays, people are still waiting for a portable 60-GHz device. The power consumptions of current CMOS millimeter-wave radios are of Watt-levels therefore hinders the 60-GHz radio to get into mobile devices. Researchers are investigating mW-level 60-GHz radio, and the receiver front end becomes the critical part. Furthermore, the modeling inaccuracy and PVT variations cause issues for moving forward from research prototypes to manufacturable products. In this dissertation, multi-dimensional aspects of issues for designing critical building blocks are discussed as follows:

- A systematic modeling methodology is proposed for both passive components and active devices in CMOS technologies for millimeter-wave design. The modeling methodology provides an efficient way to establish the required

model set for facilitating first-pass mmW silicon. The modeling methodologies are validated by measurements of 65-nm CMOS test structures.

- A 60-GHz low-noise amplifier with 15% fractional bandwidth provides full coverage of the FCC 60-GHz band (57-64 GHz). The broadband LNA, fabricated in standard 90-nm CMOS technology, features a proposed temperature-compensation biasing technique, which confines the gain variation within 5 dB for temperature variation from -5 to 85 ^{o}C. The measured gain and NF are 21 and 6.5 dB, respectively, for 49-mW power dissipation. An LNA design methodology against modeling inaccuracies is also proposed. The broadband LNA with 23% fractional bandwidth keeps a reasonable performance with nominal gain and NF of 20 and 5 dB, respectively, for a wide range of model parameters assuming a low-accuracy model is used and verified by post-layout simulation.
- The inherent bimodal oscillation phenomenon of QVCOs usually used as the IF frequency source is investigated in detail. The numerical analysis reveals that the tendency of oscillation modes is affected by the initial condition of the LC tank when oscillation starts. By exploiting this observation, a systematic measurement technique is proposed to characterize the oscillation behavior of the QVCO and verified on a 13-GHz QVCO in 90-nm CMOS. Furthermore, the proposed technique can be utilized to extend the tuning range of the QVCO, which possesses dual tuning curves with no penalties on phase noise. The measured tuning range of the QVCO is 21.4%, which is able to be continuously

tuned from 11.7 to 14.5 GHz with no gaps in between. The measured phase noise is -107.8 dBc/Hz at 1 MHz offset with power consumption of 10.8 mW.

- A millimeter-wave VCO is designed and fabricated in 65-nm CMOS. The 41.6-47.4 GHz VCO provides a fractional tuning range of 13%. The mm-wave VCO is fully characterized against voltage stress. HCI effects for reliability issues are investigated, which is a novel interdisciplinary research area.
- The mm-wave VCO is further integrated into an mm-wave down converter, which down converts the mm-wave RF signal from the LNA to IF. Power consumption is a critical bottleneck for previous integrated down converter design because the mixer requires sufficient LO power, and therefore lots of power is dissipated by the LO buffer amplifier to compensate the path loss between the VCO and the mixer. This design integrates the VCO and the mixer in an elegant floor plan where the power-consuming LO buffer amplifiers can be neglected. Conversion loss of 1.4 dB is obtained with total power consumption of 72.5 mW in 65-nm CMOS.
- A power-management system consisting of low-dropout regulators is designed in 90-nm CMOS to provide a stable and low-noise supply voltage for mm-wave receiver front end. The LDOs are measured to sustain output voltages of 1 and 1.2 V over various temperatures, input voltages, and output current conditions. The power-management system is integrated into a 90-nm CMOS 60-GHz radio and the quiescent current of each LDO is 620 μA.

7.2 Future Work

The key components for mm-wave receiver front end, including LNA, frequency generation circuits for mm-wave LO and IF, and mixer, are developed in this dissertation. In addition, power management circuits are also designed to provide controllable supply voltage. With these building blocks for a low power and manufacturable mm-wave receiver front end, the obvious potential future work is integration for a monolithic receiver front end. In addition to that, this research work can be extended into the following areas in the future for performances improvements:

- Improvements on power consumption reduction: One of the goals of this dissertation is to implement low power CMOS millimeter-wave receiver front-end building blocks. It is achieved for most components, but there is still, technically, room for improvement. For example, the tuning range of the VCO can be segmented by switch capacitor bank. Therefore, smaller varactors with better quality factors can be used. The overall tank quality factor is thus increased as well, which implies less loss that needs to be compensated by the cross-coupled pair negative impedance generator. Consequently, the current can be reduced for the negative impedance generator and power consumption can be improved.
- Optional integration of phase-locked loop (PLL) for the mm-wave VCO: PLL provides a feedback loop to stabilize the VCO output frequency. In the phase noise measurement for mm-wave VCO in Section 5.3.2, it is due to the wide tuning range of the VCO that the measured phase noises reveal a large deviation of 5 dB. If a PLL is integrated, the phase noise can be measured in

higher accuracies. A simpler alternative is to integrate the mm-wave frequency divider with the VCO instead of completing the PLL loop on chip. After the output frequency is divided low enough to be processed by off-the-shelf PLL ICs, the feedback loop can be closed on the board for measurements.

- Digital calibration circuits for "self-healing" mm-wave receiver front end: This dissertation emphasizes on the effects of modeling inaccuracy and PVT variation and develop methods to alleviate the effect. A more aggressive approach is to adjust the circuit automatically after fabrication to react the imperfections, which is the concept of "self-healing". Several self-healing methods for RF front end circuits at low frequency have been published [20]-[21], but are not applicable to mm-wave yet. A self-healing mm-wave transceiver, which provides loop-back control unit for on-chip self-testing capability, is the next step for a manufacturable mm-wave radio.
- Ultra low-power receiver front end for beam-forming phased-array system: As mentioned in Section 2.1.2 and 2.2.5, the 60-GHz channel is very lossy. To compensate the loss and to exploit the antenna size advantage at millimeter-wave frequencies, high gain antennas can be used, but also results in narrow-beam, highly-directive antenna patterns. Beam-forming phased-array system broadens the coverage and enables NLOS link. Nevertheless, the overhead of power consumption is also multiplicative. It is very challenging, but necessary, to design an ultra low-power mm-wave receiver front end to facilitate mW-level phased-array system that can be powered by batteries.

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